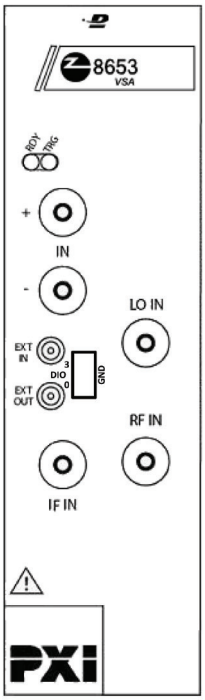
8653 VSA

TECHNICAL SPECIFICATIONS

z8653
Signal Analyzer
PXIe

LITEPOINT

Front Panel



Label	Type	Description
IN +,-	SMA	Differential baseband input
IF IN	SMA	Single-Ended IF input
RF IN	SMA	RF input signal
LO IN	SMA	Local Oscillator input
EXT IN	SMB	External input for trigger or reference
EXT OUT	SMB	External output for trigger, reference or event
DIO[1]	Header, 8-pin	Digital input/output, 4-signal (e.g. MIPI, SPI, I2C)

[1] DIO connector available on product revision 1B and later.

RF Input Channel

Specification	Value
Channel	Quantity 1
Input Impedance	50 Ω ≤ ±1% accuracy
Input VSWR (Pre-Amp On)[2] ** 250 MHz to 1.0 GHz 1.0 GHz to 2.0 GHz 2.0 GHz to 3.0 GHz 3.0 GHz to 4.0 GHz 4.0 GHz to 5.0 GHz 5.0 GHz to 6.0 GHz Input VSWR (Pre-Amp Off – Bypass) ** 250 MHz to 1 GHz 1.0 GHz to 2.0 GHz 2.0 GHz to 3.0 GHz 3.0 GHz to 4.0 GHz 4.0 GHz to 5.0 GHz 5.0 GHz to 6.0 GHz	 ≤ 1.9:1 (-10.0 dB RL) Typ ≤ 1.6:1 (-12.5 dB RL) Typ ≤ 1.5:1 (-14.0 dB RL) Typ ≤ 1.5:1 (-14.0 dB RL) Typ ≤ 1.5:1 (-14.0 dB RL) Typ ≤ 1.4:1 (-15.0 dB RL) Typ ≤ 1.9:1 (-12.0 dB RL) Typ ≤ 1.3:1 (-17.0 dB RL) Typ ≤ 1.6:1 (-12.5 dB RL) Typ ≤ 1.4:1 (-15.5 dB RL) Typ ≤ 1.6:1 (-12.5 dB RL) Typ ≤ 1.4:1 (-15.5 dB RL) Typ
Attenuator & Preamplifier Stages[3] RF Attenuator #1 (electronic) RF Preamplifier (electronic) RF Attenuator #2 (electronic) IF Attenuator #3 (electronic)	 0 – 31.5 dB attenuation, 0.5 dB steps 0 or 20 dB gain 0 – 31.5 dB attenuation, 0.5 dB steps 0 – 31.5 dB attenuation, 0.5 dB steps
Typical Attenuator #1 & Preamp Configuration[4] Preamp Bypassed Preamp Enabled	Reference Level: ≥ 0 dBm <0 dBm
Connectors	SMA

[2] See Figures 1A and 1B for a plot of RF input return loss with first stage Attenuator #1 settings.
[3] See Figure 2 for a simplified block diagram of RF path showing programmable attenuator and preamplifier stages.
[4] The automatic attenuation mode will optimize the programmable amplifier and attenuator settings for balanced noise and distortion performance using the frequency-dependent level calibration data. User programmable minimum Attenuator #1 setting is also available to limit VSWR effects.

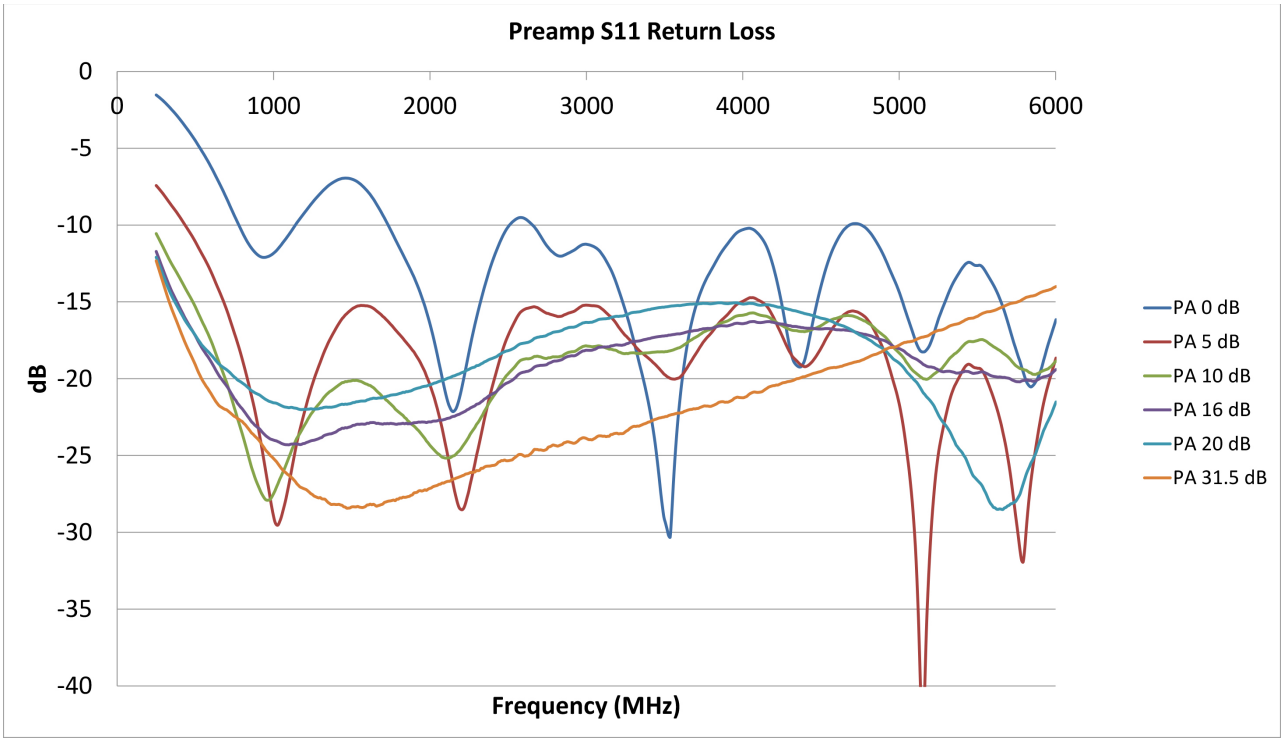


Figure 1: Typical RF Input Return Loss (RL) with Pre-Amp (PA) On vs ATT1

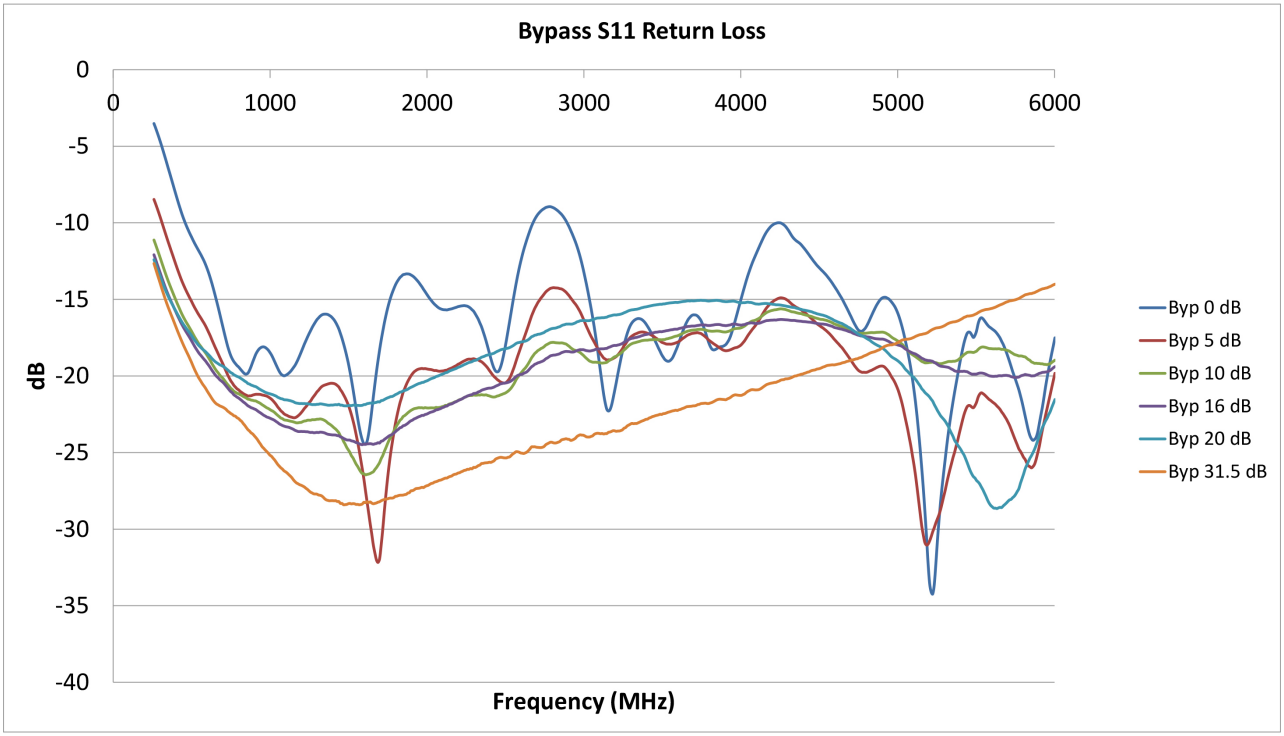


Figure 2: Typical RF Input Return Loss (RL) with Pre-Amp Off (Bypass) vs ATT1

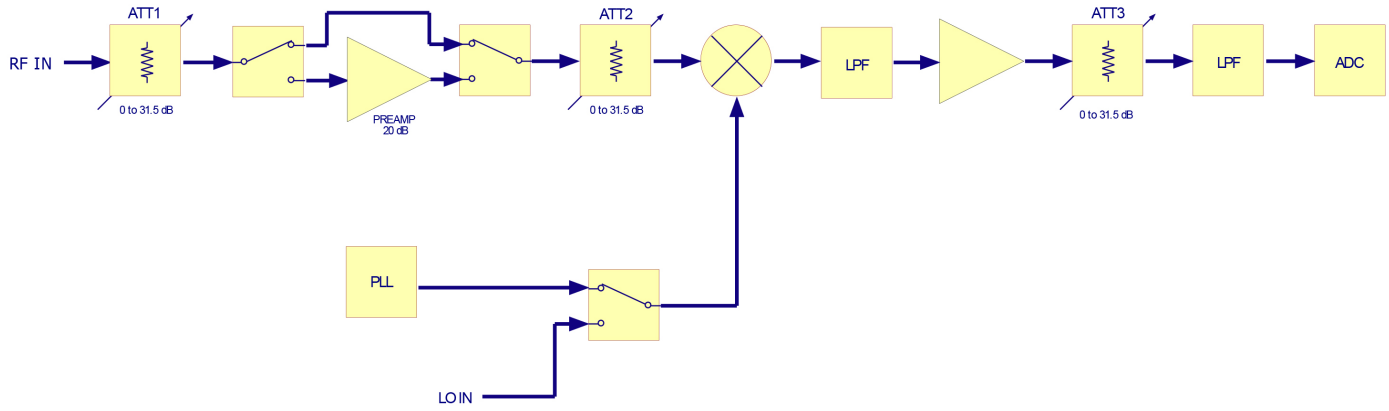


Figure 3: Simplified Block Diagram Showing Attenuator and Preamplifier Stages

RF Input Reference Level

Specification	Value
Absolute Maximum Input (no damage) Preamplifier Bypassed Preamplifier Enabled	 +30 dBm +10 dBm (ABSOLUTE MAX)
Reference Level Range (set for average power)[5]	-50 dBm to +20 dBm
Reference Level Accuracy (at 25 °C ambient, -50 to +20dBm, 540 MHz IF, IF1)	≤ ±0.5 dB ≤ ±0.1 dB typical for 1-6 GHz
Reference Level Temperature Drift **	-0.03 dB/°C
Reference Level Switching Speed	≤ 1 ms, any level change

RF Input Frequency

Specification	Value
Input Frequency Range	250 MHz to 6 GHz
Input Frequency Resolution	1 Hz
Input Frequency Switching Speed	≤ 1 ms, any frequency change

[5] Assumes crest factor of +10 dB. Peak Envelope Power (PEP) is 10 dB higher than average power, and the ADC full-scale range provides ~10 dB of headroom above the selected Reference Level for RF input.

RF Input – IF Bandwidth

Specification	Value
IF Instantaneous Bandwidth (IFBW)	81.25% of sample rate 1.015 GHz, 507 MHz, or 253 MHz to 100 Hz, 1 Hz resolution
Resolution Bandwidth	1 Hz to 3 MHz 0.1 Hz resolution
IF Path Bandwidth IF1 (default/recommended) IF2 IF3	 40 to 1000 MHz, 540 MHz center 40 to 120 MHz, 55 MHz center 250 to 1000 MHz, 540 MHz center
IFBW Flatness IF1: +/- 500MHz IF WLAN VHT80 Channel Frequencies WLAN VHT160 Channel Frequencies Note: Measured with VSG z8751 in loopback no compensation	 ≤ ±3 dB ≤ ±0.5 dB (Typ: ±0.25 dB) ≤ ±0.5 dB (Typ: ±0.25 dB)

Recommended RF/IF Settings

RF Frequency/Test Case	IF1 Center Frequency	Span
250 MHz to 354 MHz 355 MHz to 440 MHz 441 MHz to 750 MHz 751 MHz to 6 GHz	1 GHz 900 MHz 800 MHz 540 MHz	≤ 253 MHz ≤ 253 MHz ≤ 253 or 507 MHz ≤ 253, 507, or 1015 MHz
For EVM Testing: Internal or dual external LO 751 MHz to 6 GHz Shared external LO: 751 MHz to 6 GHz	 540 MHz 180 MHz	 ≤ 253 MHz ≤ 253 MHz
For Mask Testing 11a/b/g/n 11ac 20/40 MHz 11ac 80 MHz 11ac 160 MHz	 540 MHz 540 MHz 540 MHz 540 MHz	 120 MHz or 3X modulation BW 120 MHz or 3X modulation BW 253 MHz 507 MHz

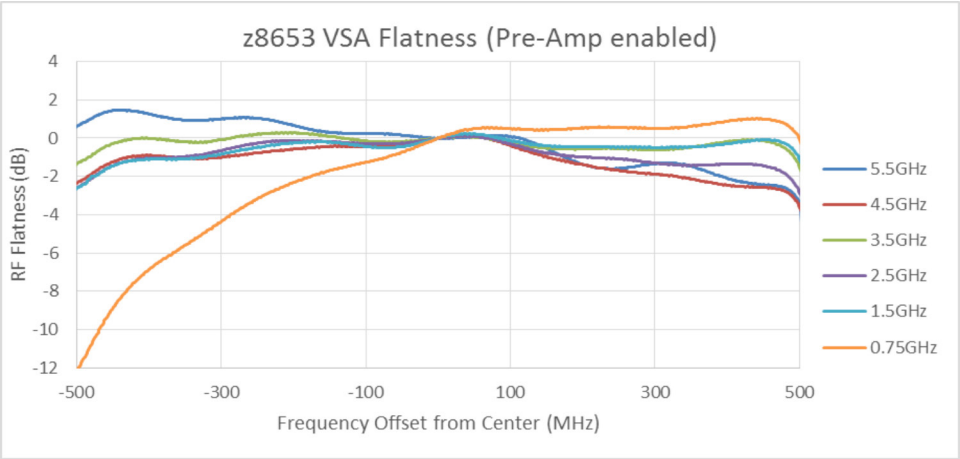


Figure 4: z8653 RF Flatness 250 MHz to 6 GHz – Pre-Amp enabled (<0dBm Ref Level)

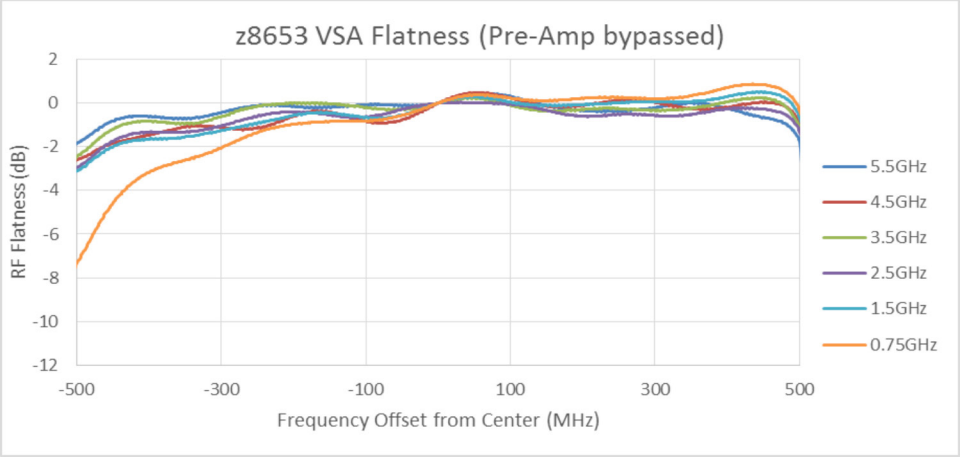


Figure 5: z8653 RF Flatness 250 MHz to 6 GHz - Pre-Amp disabled (≥0dBm Ref Level)

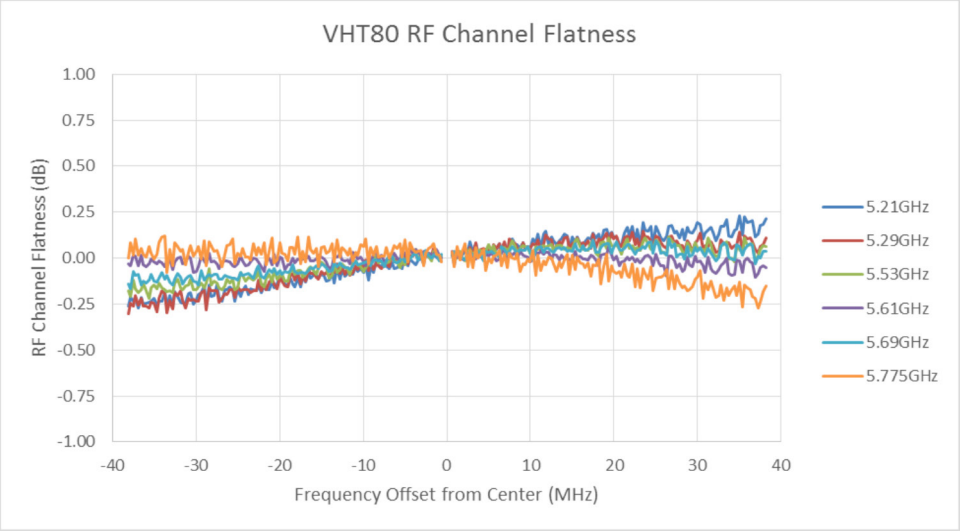


Figure 6: Typical WLAN VHT80 RF Channel Flatness

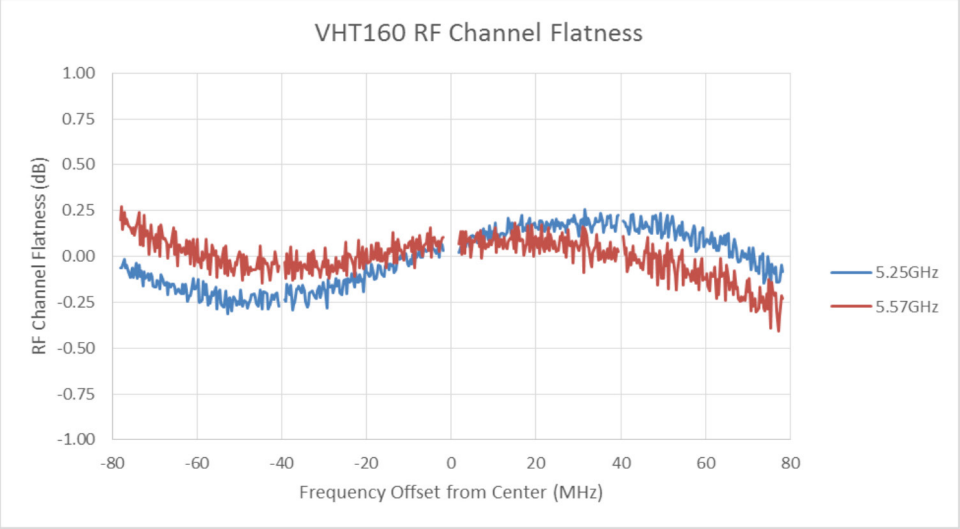


Figure 7: Typical WLAN VHT160 RF Channel Flatness

RF Input Dynamic Performance

Specification	Value
Spurious-Free Dynamic Range (excluding harmonics)	≥ 75 dBc 0 dBm Reference Level
Third-Order Intermodulation Distortion (IMD3)[6]	≥ 60 dBc
RF Input Harmonics	≤ -40 dBc

Displayed Average Noise Level (DANL)

Reference Level	Value
0 dBm	-144 dBm/Hz
-10 dBm	-153 dBm/Hz
-20 dBm	-161 dBm/Hz
-30 dBm	-162 dBm/Hz
-40 dBm	-163 dBm/Hz
-50 dBm	-163 dBm/Hz

Note: Measured at 1.8, 2.4, & 5.8 GHz

Phase Noise, Single Sideband, PXIe (Max)

Offset	1.0 GHz	2.4 GHz	5.8 GHz
1 kHz	-99 dBc/Hz	-92 dBc/Hz	-85 dBc/Hz
10 kHz	-113 dBc/Hz	-104 dBc/Hz	-97 dBc/Hz
100 kHz	-124 dBc/Hz	-117 dBc/Hz	-109 dBc/Hz
1 MHz	-137 dBc/Hz	-133 dBc/Hz	-129 dBc/Hz

[6] See Figures 3 and 4 for plots of the noise and distortion tradeoff versus input power for a fixed Reference Level setting (with preamplifier bypassed and enabled).

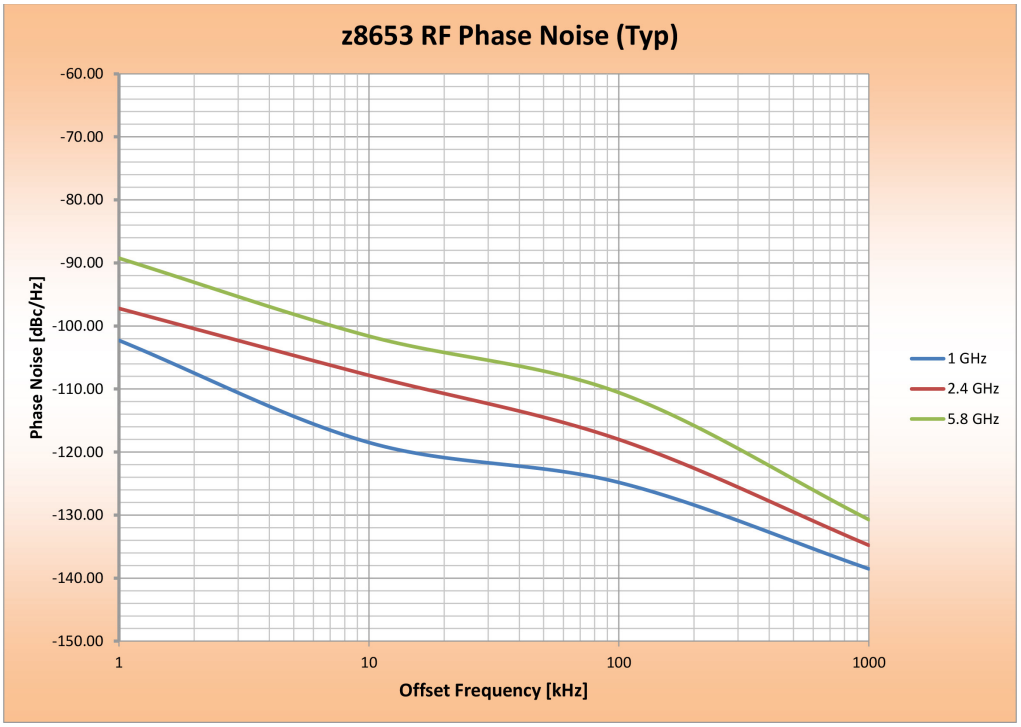


Figure 8: Typical Phase Noise

Local Oscillator Input

Local Oscillator (LO) Input Channel

Reference Level	Value
LO Input Channel	Quantity 1
Input Impedance	50 Ω
Connector	SMA
Input Level	+4 dBm nominal, ±2 dB
Absolute Maximum Input	+10 dBm
Frequency Range	250 MHz to 6.55 GHz

Timebase Reference

Reference Level	Value
Timebase Reference	10 MHz or 100 MHz
Timebase Reference Source	Internal TCXO, External Input, Backplane CLK10 or CLK100 (PXIe)
Internal TCXO Timebase	±2.5 ppm accuracy
Timebase Output	External Output

Baseband Inputs

Differential Baseband Input Channel (IN+/-)

Reference Level	Value
Channel	One Differential Input, IN+/-
Input Impedance Single-ended Differential	 50 Ω 100 Ω ≤ ±1% accuracy
Input VSWR ** 10 kHz to 460MHz 460 MHz to 1 GHz	 ≤ 1.9:1 (R.L. < -10dB) Typical ≤ 3.5:1 (R.L. < -5dB) Typical
Input Bias Current **	≤ ±10 µA
Connectors	SMA
Absolute Maximum Input (no damage) Single-ended	 -2 V to +5 V (DC + peak AC), CAT I
Input Voltage Range	+4 dBm (1 Vppd)
Input Voltage Range Accuracy (500 MHz)	≤ +0.1 / -0.3 dB at 25 °C ambient ≤ ±0.03 dB drift per °C
Input Offset Adjustment	No adjust
Analog Bandwidth -3 dB Bandwidth Stopband Rejection	 10 kHz to 1.015 GHz ≥80 dB at 2 GHz
Passband Flatness 10 kHz to 50 MHz 10 MHz to 800 MHz 10 kHz to 1.015 GHz	 +0.2 / -0.2 dB +0.5 / -1.0 dB +0.5 / -3.0 dB

Single-Ended IF Auxiliary Input Channel (IF IN)

Reference Level	Value
Channel	One Single-Ended Input, IF IN
Input Impedance	50 Ω ≤ ±1% accuracy
Input VSWR ** 20 MHz to 575 MHz 575 MHz to 1 GHz	 ≤ 1.9:1 (R.L. < -10 dB) Typical ≤ 1.44:1 (R.L. < -15 dB) Typical
Input Bias Current **	≤ ±1 nA (AC coupled)
Connector	SMA
Absolute Maximum Input (no damage)	±2 V (DC + peak AC), CAT I
Input Voltage Range	+4 dBm (1 Vpp)
Input Voltage Range Accuracy (500 MHz)	≤ +0.1 / -0.3 dB at 25 °C ambient ≤ ±0.03 dB drift per °C
Analog Bandwidth -3 dB Bandwidth Stopband Rejection	 10 MHz to 1.015 GHz ≥ 80 dB at 2 GHz
Passband Flatness 40 MHz to 50 MHz 40 MHz to 750 MHz 40 to 1.015 GHz	 +0.25 / -1.0 dB +0.75 / -1.4 dB +0.75 / -3.0 dB

Input Dynamic Performance (IN+/- and IF IN)

Reference Level	Value
Spurious-Free Dynamic Range (Excluding harmonics) (Tested at 10.7, 60.1 and 250MHz)	≥ 73 dBc Typical
Harmonic Distortion	≥ 74 dBc at 250 MHz
Intermodulation Distortion (2 tone, 20±1, 251±1, 500±1, 750±1, & 1000±1 MHz)	≥ 73 dBc Typical
Average Noise Density IN +/- IF	 ≤ -138 dBm/Hz ≤ -143 dBm/Hz
Phase Noise (187.5 MHz, typical) 1 kHz offset frequency 10 kHz offset frequency 100 kHz offset frequency 1 MHz offset frequency 10 MHz offset frequency	 -115 dBc/Hz -134 dBc/Hz -139 dBc/Hz -139 dBc/Hz -140 dBc/Hz

Analog-to-Digital Converter (ADC) & Digital Downconverter (DDC)

Reference Level	Value
ADC Vertical Resolution	12 Bits 0.024% of full-scale range
ADC Clock Frequency	2.5 GS/s sampling
ADC Clock Jitter **	≤ 150 fs RMS
I/Q Data Vertical Resolution[7]	up to 32 bits 16-bit and 32-bit data formats
I/Q Data Rate (flexible data rate with fractional resampling)	123 S/s to 312.5 MS/s, 612.5 MS/s, & 1.25 GS/s 2.5 GS/s (DDC Bypass) 1 Hz resolution
I/Q Data Memory	512 MiByte total
I/Q Waveform Size (matched I/Q sizes)	up to 128 MiSamples (16-bit data) up to 64 MiSamples (32-bit data for ≤312.5MS/s sample rate)
Input Channel Mode (DDC input feed)	RF input Baseband IN+/- input IF IN input
Baseband/IF Instantaneous Bandwidth (alias-free)	81.25% of sample rate (DDC enabled) 1.015 GHz, 507 MHz, or 253 MHz to 100 Hz, 1 Hz resolution
Baseband/IF Resolution Bandwidth	1 Hz to 3 MHz 0.1 Hz resolution
Baseband/IF Center Frequency	0 Hz to 1.25 GHz 1 Hz resolution

[7] DDC filtering of quantization noise adds to vertical resolution by 10*log10(OSR), where OSR is the oversampling ratio. For example, DDC filtering from 2.5 GS/s to 625 MS/s provides 10*log10(2500/625)=6 dB, or 1 bit additional resolution.

WLAN Modulation Analysis

IEEE 802.11a/g/n/ac OFDM

Residual EVM (Typical), Internal LO with 540 MHz IF offset on VSA, z8751 signal source

Modulation Bandwidth	RF Input Frequency: 2.4 GHz to 2.5 GHz[8] RF Input Reference Level: -30 dBm to +5 dBm	
	preamble only	preamble, pilot & data
20 MHz	-50 dB (0.32%)	-51.5 dB (0.26%)

Modulation Bandwidth	RF Input Frequency: 5 GHz to 6 GHz[9] RF Input Reference Level: -30 dBm to +5 dBm	
	preamble only	preamble, pilot & data
20 MHz	-44.5 dB (0.60%)	-46.5 dB (0.47%)
40 MHz	-43.5 dB (0.67%)	-47 dB (0.45%)
80 MHz	-42.5 dB (0.75%)	-46.5 dB (0.47%)
160 MHz	-41 dB (0.89%)	-45 dB (0.56%)

Residual EVM (Typical), Shared External LO using z8801 with 180 MHz IF offset on VSA & z8751 VSG

Modulation Bandwidth	RF Input Frequency: 2.4 GHz to 2.5 GHz[10] RF Input Reference Level: -30 dBm to +5 dBm	
	preamble only	preamble, pilot & data
20 MHz	-52 dB (0.25%)	-56.5 dB (0.15%)

Modulation Bandwidth	RF Input Frequency: 5 GHz to 6 GHz[11] RF Input Reference Level: -30 dBm to +5 dBm	
	preamble only	preamble, pilot & data
20 MHz	-52 dB (0.25%)	-56 dB (0.16%)
40 MHz	-50.5 dB (0.30%)	-53.5 dB (0.21%)
80 MHz	-48 dB (0.40%)	-51.5 dB (0.26%)
160 MHz	-45 dB (0.56%)	-48 dB (0.40%)

[8] Excluding channel center frequency of 2.467 GHz
[9] Excluding channel center frequencies of 4.99 GHz, 5.25 GHz, 5.69 GHz
[10] Excluding channel center frequency of 2.467 GHz
[11] Excluding channel center frequencies of 4.99 GHz & 5.69 GHz

Residual EVM (Typical), Dual LO using two z8801 with 540 MHz offset on VSA and 180 MHz offset on z8751 VSG

Modulation Bandwidth	RF Input Frequency: 2.4 GHz to 2.5 GHz[10] RF Input Reference Level: -30 dBm to +5 dBm	
	preamble only	preamble, pilot & data
20 MHz	-54 dB (0.21%)	-55.5 dB (0.17%)

Modulation Bandwidth	RF Input Frequency: 5 GHz to 6 GHz[11] RF Input Reference Level: -30 dBm to +5 dBm	
	preamble only	preamble, pilot & data
20 MHz	-53.5 dB (0.21%)	-55.5 dB (0.17%)
40 MHz	-51 dB (0.28%)	-54 dB (0.20%)
80 MHz	-49.5 dB (0.34%)	-51.5 dB (0.27%)
160 MHz	-46 dB (0.50%)	-48.5 dB (0.38%)

Center Frequency Tracking

Reference Level	Value
Frequency Range	± 625 kHz
Frequency Error	± 10 Hz + (reference accuracy X center frequency)

Trigger

Reference Level	Value
Trigger Source	I, Q, Envelope, External Input, DIO, Pattern, Software, Immediate (no trigger), TTL Trigger 0-7, Star Trigger
Trigger Slope/Polarity	Positive or Negative
Trigger Position	Pre-Trigger & Post-Trigger
Trigger Jitter	≤ 2.5 ns peak-to-peak
Trigger Resolution	Signal Triggers: Minimum 3.2ns @ $F_{SAMPLE} \geq 312.5MHz$, else $1/(F_{SAMPLE})$
Trigger Hysteresis (time)	Defines trigger hold-off time 0 to 209 µs
Trigger Hysteresis (amplitude)	Trigger hysteresis in percentage or volts

External Input (front panel)

Reference Level	Value
Functionality	Trigger Input, Timebase Reference Input
Absolute Maximum Input (no damage)	≤ ± 5 V (DC + peak AC), CAT I
Input Trigger Level Adjustment	-2 V to +2 V 0.5 mV resolution ≤ 20 mV accuracy 20 mV overdrive (input hysteresis)
Input Bandwidth (-3 dB)	≥ 250 MHz
Input Impedance	1 MΩ || 30 pF or 50 Ω ≤ ±2% accuracy
Connector	SMB

External Output (front panel)

Reference Level	Value
Functionality	Trigger Output, Timebase Reference Output, Event Output, Programmable Clock Output, Programmable Pulse Output, Constant Level
Output Event Source	Trigger Event, Capture Complete Event, Operation Complete Event, Master Summary Status Event
Polarity	High or Low Truth
Programmable Event Pulse Width	50 ns to 163 ms
Programmable Clock	Period: 26.667 ns to 100 seconds 26.667 ns resolution 50% Duty Cycle
Programmable Pulse Pulse Repetition Interval Pulse Width	 26.667 ns to 100 seconds, 26.667 ns resolution 13.333 ns
Probe Compensation	10 kHz Clock which can be used to compensate probes
Limit Test Successful	Event pulse after each capture upon limit or mask test success
Output Level	Programmable Level: Default: +3.3V into open load Open load: 0 to +5V 50 Ω load: 0 to +4.1V Level accuracy: ±5% Output Drive: ≥ ±90 mA
Output Enable	Tri-State Output Capability

Current Sense	±90 mA current sense range Triggered or immediate capture 0.1mA resolution
Connector	SMB

Digital Input/Output (DIO) Front Panel[12]

Reference Level	Value
Functionality	4-bit bi-directional Digital I/O software programmable. Future serial interfaces such as MIPI, SPI, I^2C, etc
Programmable Clock Rate	Up to 50 MHz
Programmable Logic	≥ 5 ns resolution
Programmable Direction	Input (52 kΩ pull-up) or Output
Programmable Source/Destination	Backplane triggers, external in/out, trigger event
Output Level	Programmable Level: Default: +1.2V into open load Range: +1.2V to +3.6V into open load Level accuracy: ±5% Output Drive: ≥ ±20 mA
Output Enable	Tri-State Output Capability
Connector	8-pin Latching Header

Backplane Triggers

Reference Level	Value
Functionality	Multi-Instrument Synchronization Trigger, Event Output Signals
Triggers	TTL Trigger 0-7
Direction	Input or Output
Source	Trigger Event, Capture Complete Event, Operation Complete Event, Master Summary Status Event, Constant Level
Polarity	High or Low Truth
Programmable Event Pulse Width	50 ns to 163 ms

[12] DIO connector available on product revision 1B and later.

Traces

Reference Level	Value
Trace Channels	Quantity 8
Trace Size	Up to 512 KiSample 32-bit floating point data
Trace Feed (source)	Input Channels or Reference Channels
Trace Type	Write (Live), Average, Max Hold, Min Hold (Reference Feeds use Write Type only)
Trace Average Count	2 to 65535
Trace Data Format	Linear Magnitude, Logarithmic Magnitude, Phase, Real, Imaginary, 32-bit floating point data

Reference Waveforms

Reference Level	Value
Reference Channels	Quantity 4
Reference Storage	Non-volatile memory storage
Reference Data	32 KiSample maximum waveform size 32-bit floating point data
Reference Data Format	Linear Magnitude, Logarithmic Magnitude, Phase, Real, Imaginary, 32-bit floating point data

Markers

Reference Level	Value
Marker Channels	Quantity 2
Marker Functionality	Waveform Trace Magnitude and Frequency Markers
Marker Source	Trace 1-8
Marker Peak Search Search Methods Selectable Search Options	 Maximum, Next Maximum by Amplitude, Next Maximum Left, Next Maximum Right Absolute Threshold, Relative Excursion

Data Processing & Download

Specification	Value
Self-Calibration	Automatic internal calibration: spur cancellation
Waveform Data Formats	16-bit or 32-bit signed integer (I/Q time-domain data) 32-bit floating point (Trace or Reference data) Intel or Motorola Byte Order

Instrument Stored States

Specification	Value
Functionality	Non-volatile storage of instrument setup configuration
Stored States	30 State 0 is Reset State Power-On State programmable

Status Reporting

Specification	Value
IEEE-488.2 Device Status	Reporting Structure including Status Byte, Standard Event Registers, Questionable Registers, Operation Registers and Self-Test Status Registers

LED Indicators

Specification	Value
RDY (Ready)	OFF: Hardware Failure ON: Unit has passed power-up self-diagnostics TOGGLE: Unit has an error pending in error queue
TRG (Trigger)	OFF: Trigger event not detected ON/PULSE: Trigger complete event detected TOGGLE: Device identify enabled

PXIe Interface

Specification	Value
PXIe Slot Compatibility	PXI Standard Slot and PXIe Hybrid Slot Compatible
PXI Timing & Triggering Signals (XJ4 Connector)	PXI_TRIG[0:7] input/output PXI_STAR input PXI_CLK10 input
PXIe Timing & Triggering Signals (XJ3 Connector)	PXI_DSTARA input (unused PXI_STAR input PXI_CLK10 input

Power & Cooling

Power Supplies

Model	Platform	Voltage	Typical Current	Maximum Current
z8653	PXIe	+3.3 VDC +12 VDC	0.96 A 2.73 A	1.06 A 3.00 A

Total Cooling & Power Consumption

Model	Platform	Typical Cooling & Power	Maximum Cooling & Power
z8653	PXIe	32.8 W	36 W

Notes: Self-protect thermal shutdown will activate at ~50°C. Reset of instrument required to recover from thermal shutdown.
Recommend use of slot blockers in chassis for empty slots. Units tested in zSeries 9-slot and 18-slot chassis.

Physical & Environmental

Size & Weight

Specification	Value
Physical size	Double-Wide 3U PXIe Instrument 8.25" x 1.59" x 5.25" (L x W x H) 20.96 cm x 4.03 cm x 13.34 cm (L x W x H)
Weight	27.4 oz or 777 g

Temperature Range

Specification	Value
Operating	0°C to +40°C ambient (MIL-PRF28800F Class 3)
Storage	-40°C to +75°C (MIL-PRF28800F Class 3)
Over-Temperature	Automatic shutdown if internal temperature exceeds +50°C
Calibration Range	+20°C to +30°C ambient, after a 20 minute warm-up period, to meet all calibration specification accuracies

Relative Humidity

Specification	Value
Operating or Storage Up to +30°C +30°C to +40°C above +40 °C	 5 to 95% ± 5% non-condensing, 5 to 75% ± 5% non-condensing, 5 to 45% ± 5% non-condensing

Altitude

Specification	Value
Operating	Up to 5 km
Storage	Up to 15 km

Additional Resources

LitePoint zSeries offers several hardware and software resources. Please visit the website www.litepoint.com for the latest information and versions. Detailed information is also available in the individual manuals. Resources include: zSignal soft front panels, instrument drivers, cables and probes.

Methodology

All Specifications describe the performance at an ambient temperature of 20-25° C unless otherwise noted.

All Specifications are Factory tested to verify performance meets the specified limits, except those marked with (**) which are guaranteed by design, or those marked as Typical.

Specifications marked as Typical indicate that 80% of the units tested fall within the limits.

Terminology

Numeric Prefixes

When referring to numeric values, this document will use SI (International System of Units) and IEC (International Electrotechnical Commission) standard prefixes. Prefix definitions are in the following table.

Prefix	Multiplier
n (nano)	1/(1000x1000x1000)
µ (micro)	1/(1000x1000)
m (milli)	1/1000
k/K (kilo)	1000
M (Mega)	1000x1000
G (Giga)	1000x1000x1000
Ki (Kibi)	1024
Mi (Mebi)	1024x1024
Gi (Gibi)	1024x1024x1024

Differential Outputs

Single-Ended is used to refer to the output on either the + or – output pin

Differential is used to refer to the output between the + and- output pins

Vd indicates Volts differential

Vppd indicates Volts peak-to-peak differential

Safety

This product is designed to meet the requirements of the following standard of safety for electrical equipment for measurement, control and laboratory use: EN 61010-1

Electromagnetic Compatibility

CE Marking EN 61326-1:1997 with A1:1998 and A2:2001 Compliant

FCC Part 15 (Class A) Compliant

Emissions

EN 55011	Radiated Emissions, ISM Group 1, Class A, distance 10 m, emissions < 1 GHz
EN 55011	Conducted Emissions, Class A, emissions < 30 MHz Immunity
EN 61000-4-2	Electrostatic Discharge (ESD), 4 kV by Contact, 8 kV by Air
EN 61000-4-3	RF Radiated Susceptibility, 10 V/m
EN 61000-4-4	Electrical Fast Transient Burst (EFTB), 2 kV AC Power Lines
EN 61000-4-5	Surge
EN 61000-4-6	Conducted Immunity
EN 61000-4-8	Power Frequency Magnetic Field, 30 A/m
EN 61000-4-11	Voltage Dips and Interrupts

CE Compliance

This product meets the necessary requirements of applicable European Directives for CE Marking as follows:

73/23/EEC Low Voltage Directive (Safety)
89/336/EEC Electromagnetic Compatibility Directive (EMC)

See Declaration of Conformity for this product for additional regulatory compliance information.

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