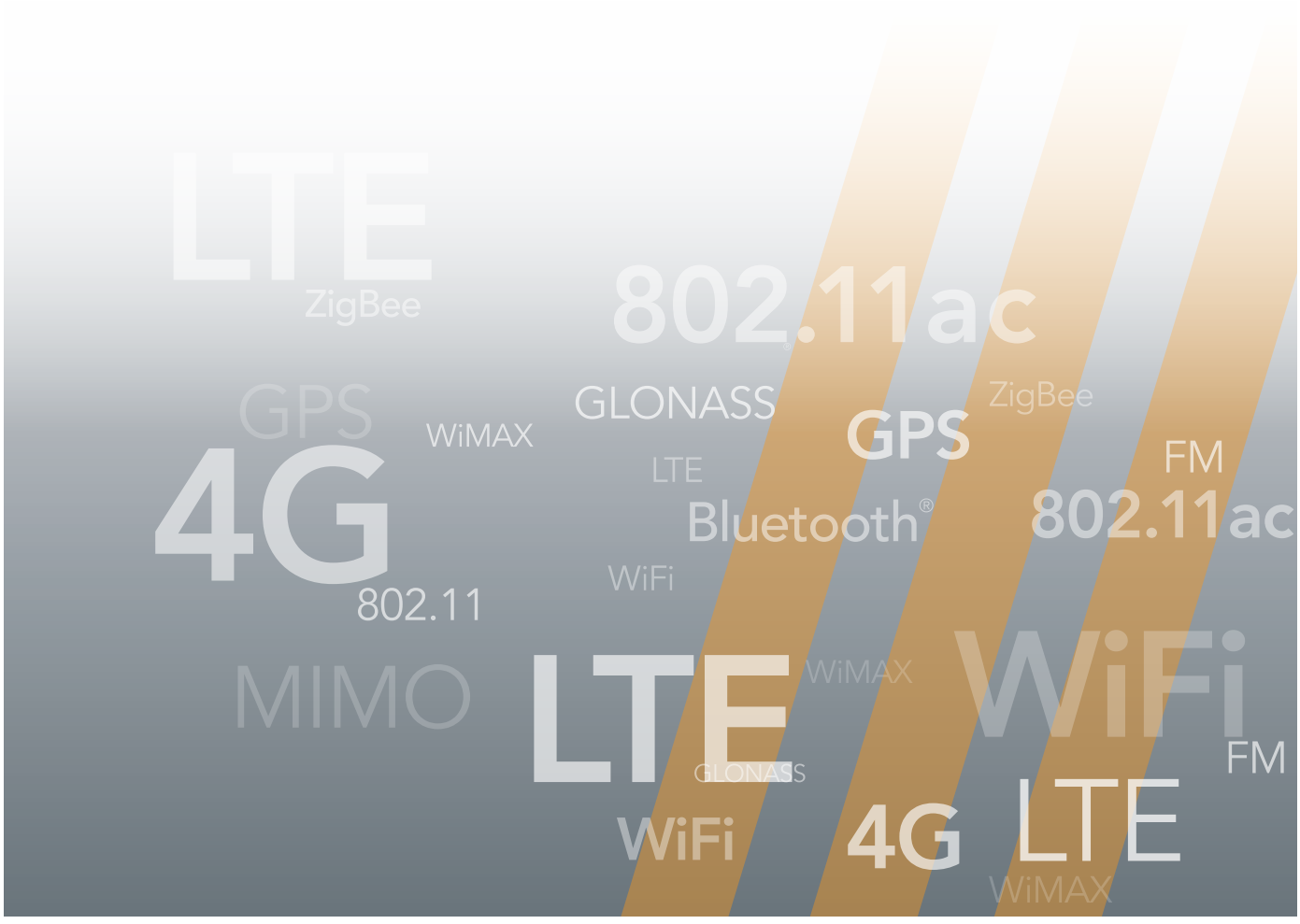
8820

TECHNICAL SPECIFICATIONS

z8820 PXIe
DC Power & Digital IO Controller



LITEPOINT

Overview

The z8820 PXIe DC Power & Digital IO Controller Module is a single-slot 3U PXIe module that supports remote instrumentation modules outside the PXI chassis such as the z8812 Port Module. The z8820 module uses a PCI Express (PCIe) Gen1 x1 lane to interface to the PXIe host computer. PCIe read/write operations provide access to the z8820 on-board resources and to digital I/O or SPI interfaces to remote instruments. The z8820 PXIe module supports up to two remote instrument interfaces via two D-sub 26-pin connectors. Each remote channel connector provides eight digital I/O (DIO) signals and three power supply rails (+6V, +9V, and -13V) for external modules. The external power supply rails have voltage/current monitors that can also be used as over/under trip protection. The z8820 also has a programmable clock generator circuit to provide up to three programmable digital clocks for the SPI master circuit and for user signals on the DIO or backplane outputs.

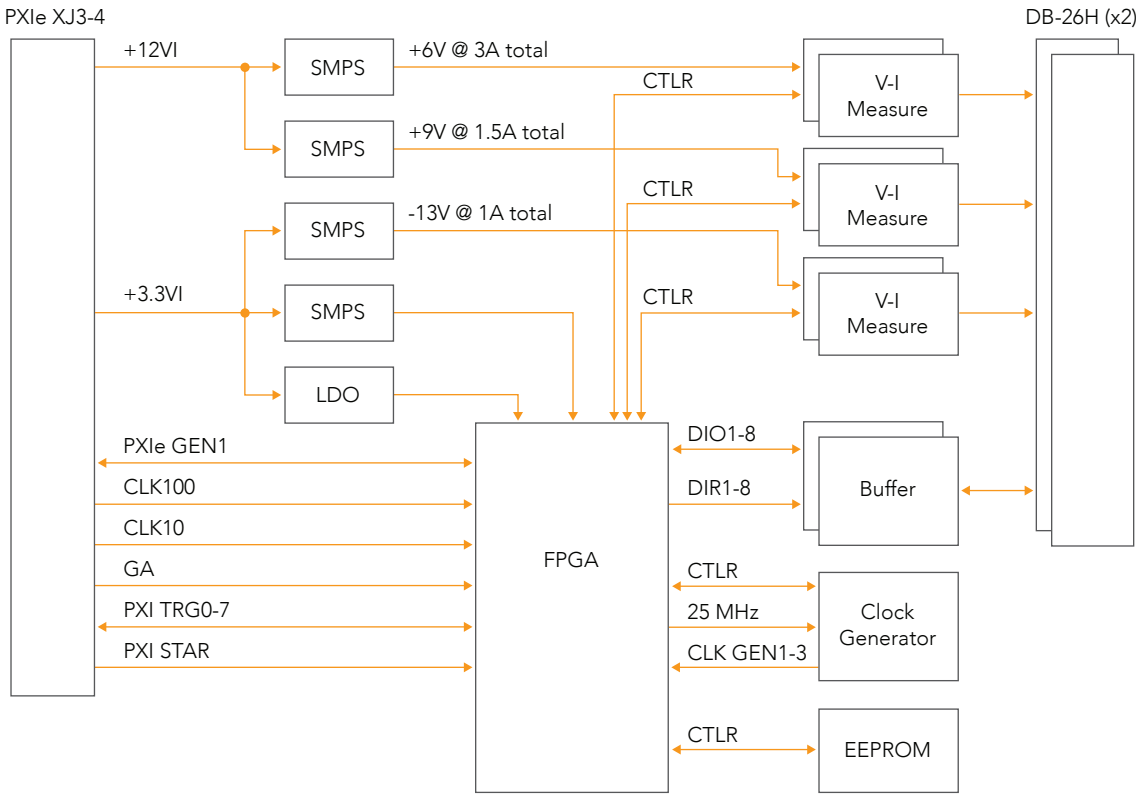


Figure 1: Block Diagram of z8820 PXIe Module

Port Descriptions

Figure 2: Front Panel of z8820 DC Power & Digital IO PXIe Module

Front Panel

Label	Type	Description
Channel 1	DB-26H	DC power supplies and digital IO control bus #1
Channel 2	DB-26H	DC power supplies and digital IO control bus #2

The z8820 PXIe uses two D-sub 26-pin triple row connectors for Channel 1 and Channel 2 interfaces. D-sub mating cables can be from 1 foot to 15 feet in length (example mating cable P/N: L-com CHD26MF).

Connector Pinout

For both channels, the pinout of the D-sub 26-pin triple row connector is identical and is shown in the following figure and table.

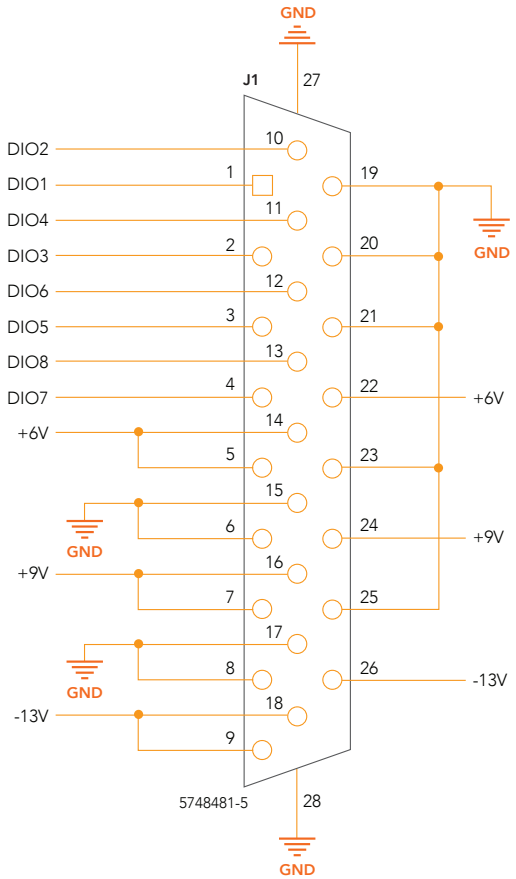


Figure 3: Front Panel Connector Pinout Diagram

Pin #	Signal Name	Type (Max Rate)	Source Imped.	Max Voltage	Nominal Voltage	Min Voltage	Max Current	Comment
1	DIO1 SPI_CLK	3.3V CMOS (52 MHz)	25Ω ± 15%	3.6 V	0 V to 3.3 V	-0.3 V	±20 mA	SPI Master Clock
10	DIO2 SPI_DWR	3.3V CMOS (26 Mbps)	25Ω ± 15%	3.6 V	0 V to 3.3 V	-0.3 V	±20 mA	SPI Master Write Data
2	DIO_D3 SPI_DRD	3.3V CMOS (26 Mbps)	25Ω ± 15%	3.6 V	0 V to 3.3 V	-0.3 V	±20 mA	SPI Master Read Data
11	DIO_D4	3.3V CMOS	25Ω ± 15%	3.6 V	0 V to 3.3 V	-0.3 V	±20 mA	
3	DIO_D5	3.3V CMOS	25Ω ± 15%	3.6 V	0 V to 3.3 V	-0.3 V	±20 mA	
12	DIO_D6	3.3V CMOS	25Ω ± 15%	3.6 V	0 V to 3.3 V	-0.3 V	±20 mA	
4	DIO_D7	3.3V CMOS	25Ω ± 15%	3.6 V	0 V to 3.3 V	-0.3 V	±20 mA	
13	DIO_D8	3.3V CMOS	25Ω ± 15%	3.6 V	0 V to 3.3 V	-0.3 V	±20 mA	
5, 14, 22	+6V	DC Power	-	6.1 V	6.0 V	5.7 V	3.0 A	1.5 A per channel
7, 16, 24	+9V	DC Power	-	9.1 V	9.0 V	8.75 V	1.5 A	0.75 A per channel
9, 18, 26	-13V	DC Power	-	-13.0 V	-13.2 V	-13.4 V	0.5 A	0.25 A per channel
6, 7, 8, 15, 17, 19, 20, 21, 23, 25	GND	Ground	-	-	0 V	-	-	

Digital Input/Output (DIO)

The z8820 PXIe module supports eight +3.3V CMOS logic DIO pins per channel (16 DIO pins total per module). The direction for each DIO pin can be set as an input or output. An output pin can be multiplexed from sources including SPI master clock and data outputs, backplane triggers, clock generator signals, and discrete register controls. An input pin can be routed to the SPI master data input, the backplane triggers, or a discrete register for reading status over the PCIe bus. The following diagram in Figure 4 shows the DIO multiplexer interface. The master SPI interface is only selectable on the first three DIO pins.

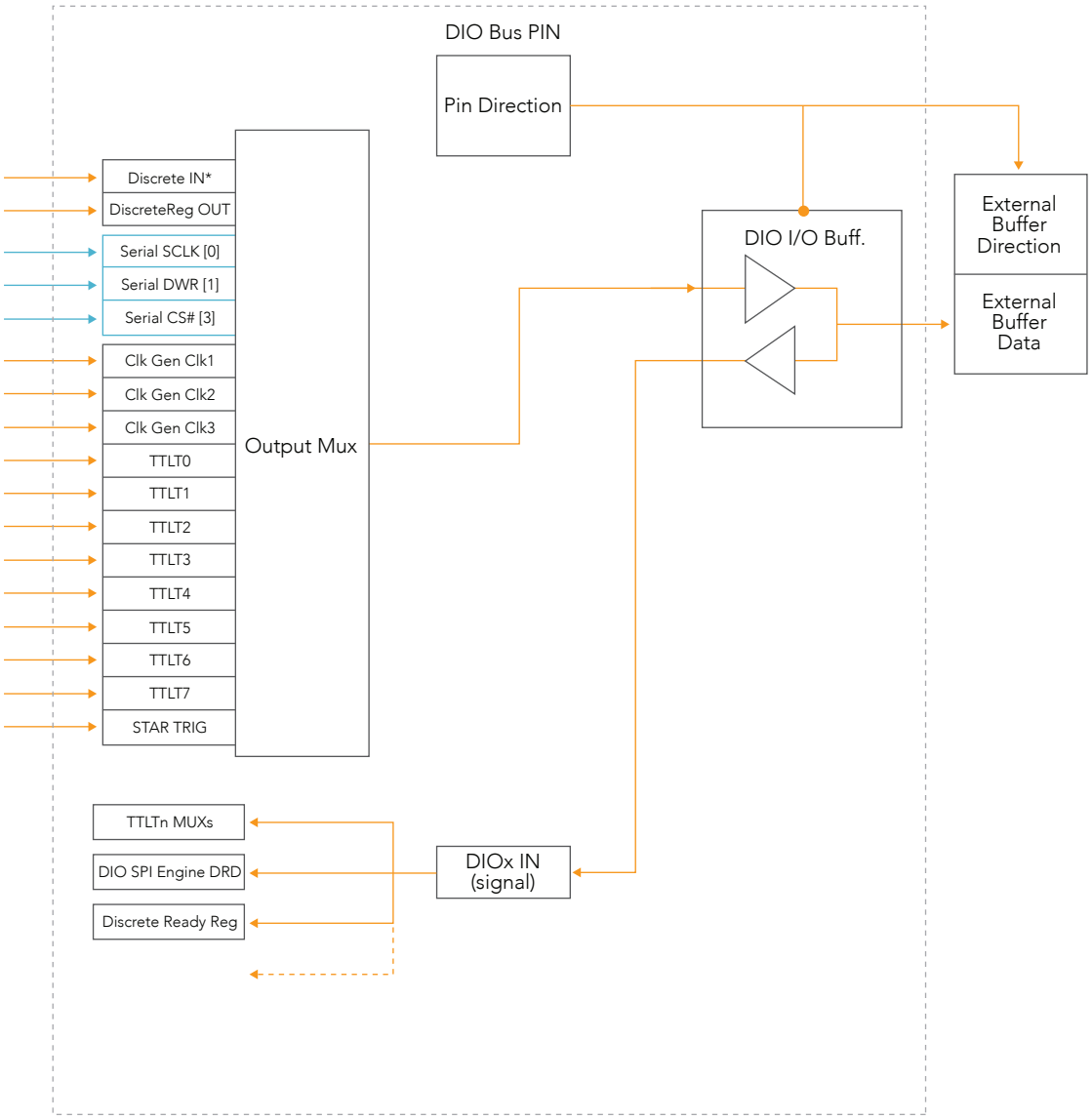


Figure 4: Digital Input/Output Pin Logic Diagram

Item	Description	Minimum	Typical	Maximum	Units
V_{Imax}	Voltage – In	-0.3		3.6	V
V_{Omax}	Voltage – Output	0.0		3.3	V
V_{IH}	Voltage – High-level Input	2.0			V
V_{IL}	Voltage – Low-level Input			0.8	V
V_{OH}	Voltage – High-level Output, IOH = -20mA	2.4			V
V_{OL}	Voltage – Low-level Output, IOL = 20mA			0.55	V
I_{OH}	Current – High-level Output			-20	mA
I_{OL}	Current – Low-level Output			20	mA
I_{I}	Current – Input (High/Low)			±2	µA
t_{PLH}	Switching – Low to High	0.7		5.8	ns
t_{PHL}	Switching – High to Low	0.8		5.0	ns
Z_{SOURCE}	Source Impedance		25		Ω
V_{ESD}	Voltage – ESD Protection	±8			kV
V_{CL}	Clamp Voltage: Positive Transients Negative Transients		 +9.2 -1.6		 V V
C_{IN}	Input Capacitance		20		pF

Master SPI Bus

The z8820 PXIe module provides a master SPI interface using a 32-bit word consisting of R/W bit, 15-bit address and 16-bit data. The data is shifted out from the master on the SPI_DWR (SPI_SIMO) wire on the negative edge of SPI_CLK, and is sampled on the rising edge of SPI_CLK. Readback data is shifted out of the remote instrument on the falling edge SPI_CLK on the SPI_DRD (SPI_SOMI) wire and is sampled by the master on the rising edge of SPI_CLK. All SPI transactions start with the MSB first.

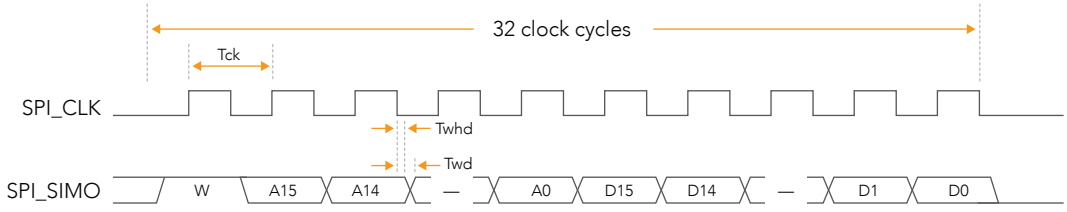


Figure 5: SPI Write Command

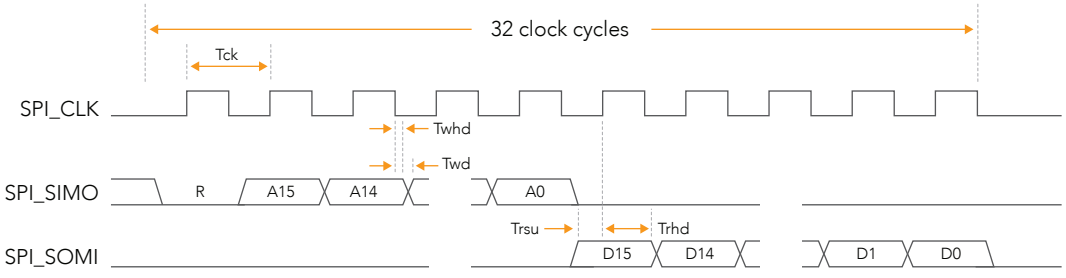


Figure 6: SPI Read Command

The SPI clock will be turned off when not transferring a command over the interface. If the remote instrument(s) require a clock to continue with post transaction operations, another DIO pin can be allocated using the same clock generator as the SPI master. By default, the SPI master uses the third programmable Clock Generator (CLK_GEN3) at a clock rate of 10 MHz. The maximum data transfer rates possible with various remote instrument cable lengths is as follows:

Cable Length	Write	Read
1 foot	26 Mbps	15 Mbps
5 feet	26 Mbps	10 Mbps
10 feet	26 Mbps	6 Mbps
15 feet	26 Mbps	5 Mbps

DC Power Supplies

The z8820 PXIe module can deliver a maximum of 38W to external instruments. This total available power is shared between up to two external instruments.

Item	Maximum Current	Maximum Delivered Power	Power-On Rise Time
+6 V Supply	3.0 A	18 W	< 75 ms
+9 V Supply	1.5 A	13.5 W	< 125 ms
-13 V Supply	0.5 A	6.5 W	< 125 ms

The z8820 PXIe module uses a maximum of 51 W of power in which up to 38 W is delivered to external instruments and the remaining 13 W is dissipated by the z8820 module. The following table shows the PXIe voltage rail loading.

Item	No Load	Typical*	Maximum
+3.3 V PXIe Current	0.25 A	2.50 A	3.25 A
+12 V PXIe Current	0.10 A	2.50 A	3.25 A
Total PXIe Power	2 W	40 W	51 W
Total PXIe Cooling	2 W	11 W	13 W

Note (*): 80% external instrument load

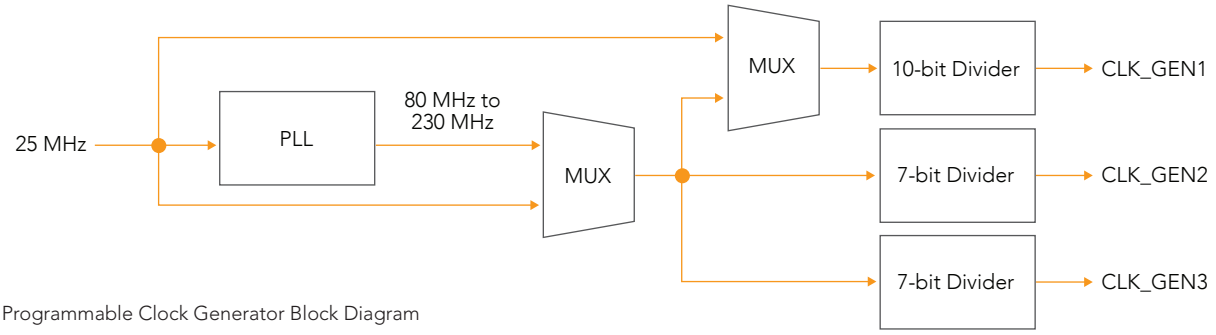


Figure 7: Programmable Clock Generator Block Diagram

Clock Generator

Item	Specification
Output Clock Rates	25 kHz to 100 MHz
Master Clock Rates	MCLKA: 25 MHz MCLKB: 80 MHz to 230 MHz, programmable
Clock Generator Signals (sourced from MCLKA or MCLKB)	CLK_GEN1: MCLKA or B with programmable 10-bit divider CLK_GEN2: MCLKA or B with programmable 7-bit divider CLK_GEN3: MCLKA or B with programmable 7-bit divider By default, CLK_GEN3 is 10 MHz and used for SPI bus
Clock Routing (CLK_GEN1-3)	DIO1-8 Channels 1-2 PXI_TRIG[0:7]

PXIe Interface

Item	Specification
PXIe Slot Compatibility	PXIe Slot and PXIe Hybrid Slot Compatible
PCI Express Interface	1 Lane, Gen 1, 2.5 Gbps
Geographical Addressing	Supported per PXIe specification 2.2.4
PXI Timing & Triggering Signals	PXI_TRIG[0:7] input/output PXI_STAR input PXI_CLK10 input PXI_CLK100 input

Physical & Environmental

Size & Weight

Item	Specification
Physical Size	Single-Wide 3U PXIe Instrument 8.25" x 0.79" x 5.25" (L x W x H) 20.96 cm x 2.01 cm x 13.34 cm (L x W x H)
Weight	6.3 oz. (178 g)

Temperature Range

Item	Specification
Operating	0°C to +40°C ambient (MIL-PRF28800F Class 3)
Storage	-40°C to +75°C (MIL-PRF28800F Class 3)

Relative Humidity

Item	Specification
Operating or Storage Up to +30°C +30°C to +40°C above +40 °C	 5 to 95% ± 5% non-condensing 5 to 75% ± 5% non-condensing 5 to 45% ± 5% non-condensing

Terminology

Numeric Prefixes

When referring to numeric values, this document will use SI (International System of Units) and IEC (International Electrotechnical Commission) standard prefixes. Prefix definitions are in the following table.

Prefix	Multiplier
n (nano)	1/(1000x1000x1000)
µ (micro)	1/(1000x1000)
m (milli)	1/1000
k/K (kilo)	1000
M (Mega)	1000x1000
G (Giga)	1000x1000x1000
Ki (Kibi)	1024
Mi (Mebi)	1024x1024
Gi (Gibi)	1024x1024x1024

Differential Outputs

Single-Ended is used to refer to the output on either the + or – output pin

Differential is used to refer to the output between the + and- output pins

Vd indicates Volts differential

Vppd indicates Volts peak-to-peak differential

Safety

This product is designed to meet the requirements of the following standard of safety for electrical equipment for measurement, control and laboratory use: EN 61010-1

Electromagnetic Compatibility

CE Marking EN 61326-1:1997 with A1:1998 and A2:2001 Compliant

FCC Part 15 (Class A) Compliant

Emissions

EN 55011	Radiated Emissions, ISM Group 1, Class A, distance 10 m, emissions < 1 GHz
EN 55011	Conducted Emissions, Class A, emissions < 30 MHz Immunity
EN 61000-4-2	Electrostatic Discharge (ESD), 4 kV by Contact, 8 kV by Air
EN 61000-4-3	RF Radiated Susceptibility, 10 V/m
EN 61000-4-4	Electrical Fast Transient Burst (EFTB), 2 kV AC Power Lines
EN 61000-4-5	Surge
EN 61000-4-6	Conducted Immunity
EN 61000-4-8	Power Frequency Magnetic Field, 30 A/m
EN 61000-4-11	Voltage Dips and Interrupts

CE Compliance

This product meets the necessary requirements of applicable European Directives for CE Marking as follows:

73/23/EEC Low Voltage Directive (Safety)
89/336/EEC Electromagnetic Compatibility Directive (EMC)

See Declaration of Conformity for this product for additional regulatory compliance information.

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