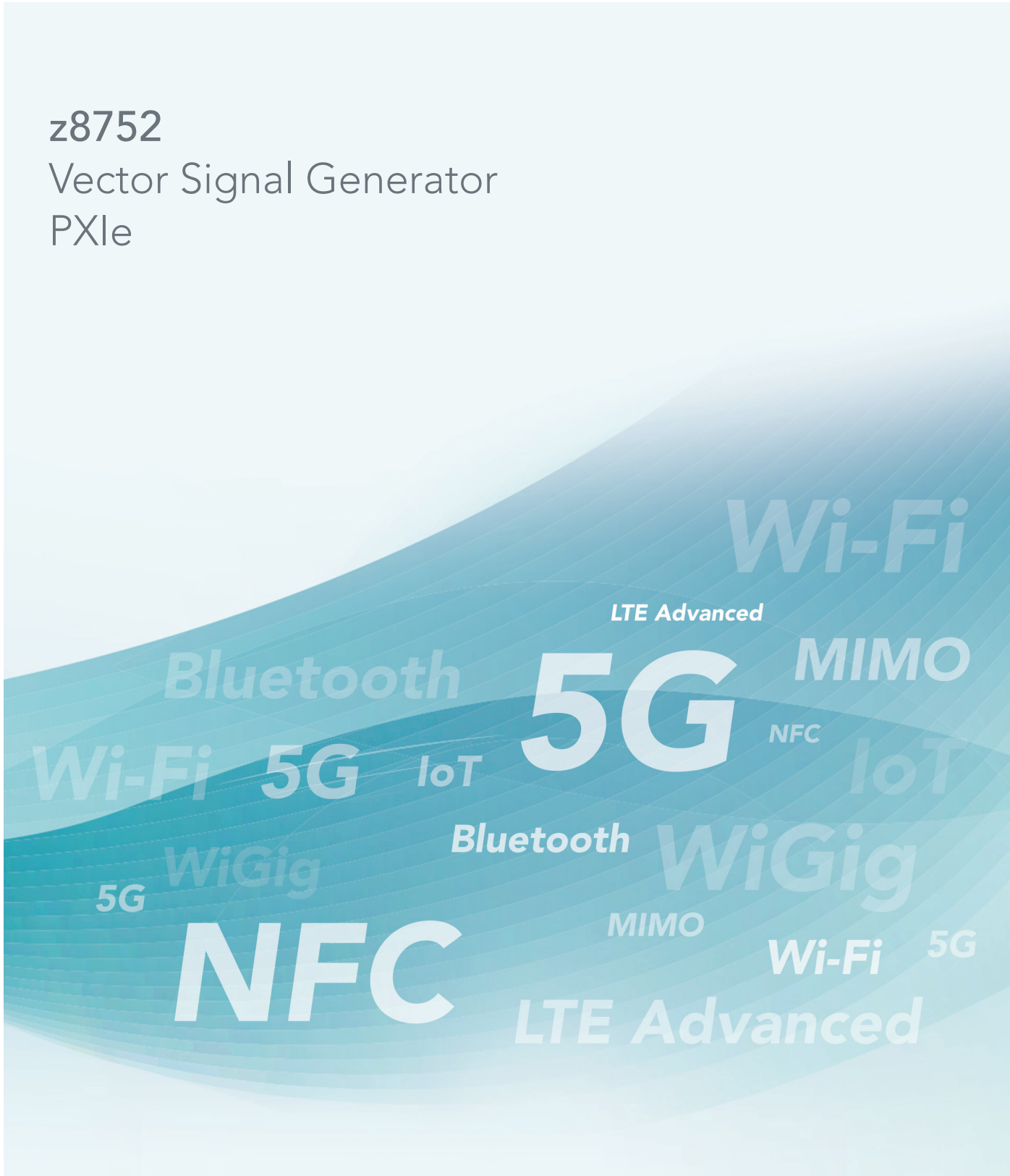


z8752
Vector Signal Generator
PXle



Front Panel



Label	Type	Description
I OUT +,-	SMA	Differential baseband I output
Q OUT +,-	SMA	Differential baseband Q output
EXT IN	SMB	External input for trigger or reference
EXT OUT	SMB	External output for trigger, reference or event
RF OUT	SMA	RF output
LO IN	SMA	Local oscillator input
DIO	Header, 8-pin, 0.05" spacing	Digital input/output, 4-signal (e.g. MIPI, SPI, I2C)

RF Output

RF Output Channel

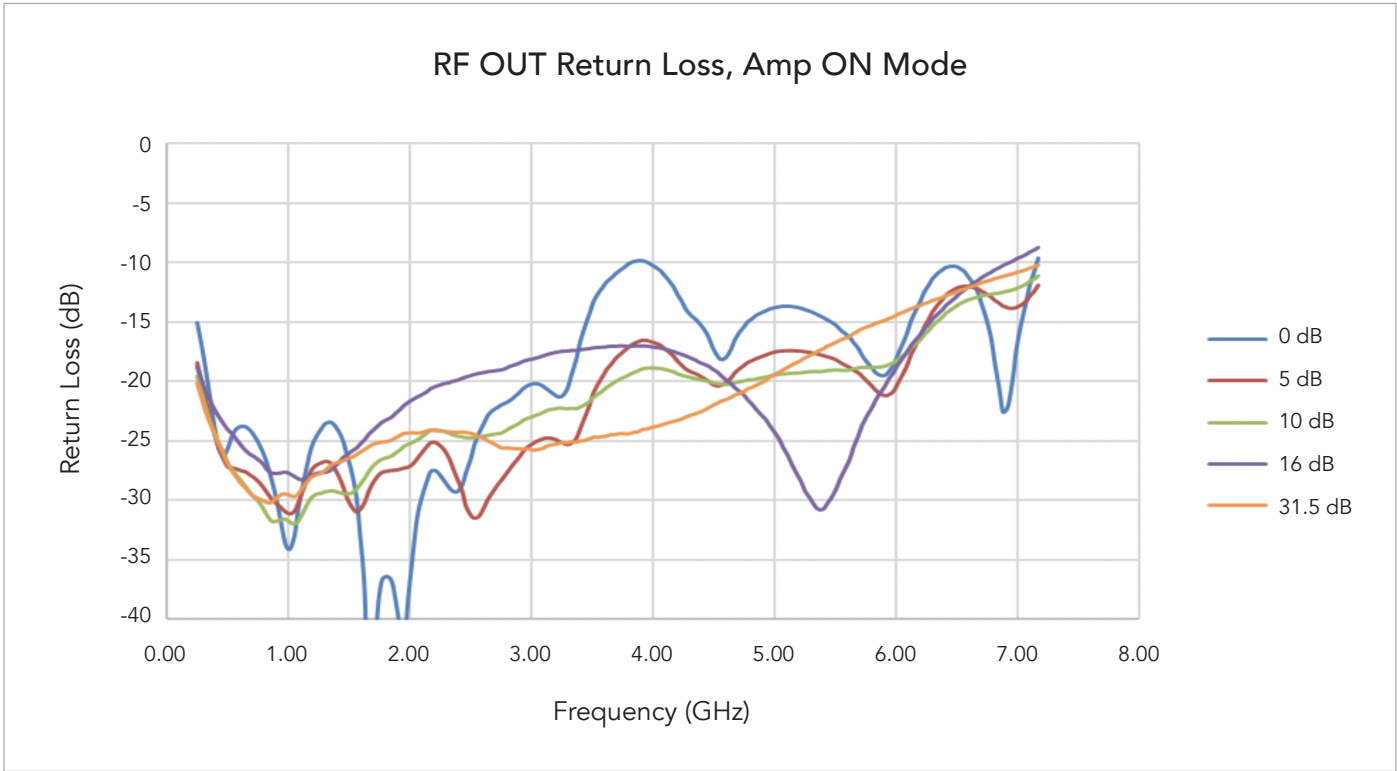
Specification	Value
RF Channel	One single-ended output, RF OUT
Output Impedance	50 Ω , nominal
Output VSWR ** (250 MHz to 7.2 GHz, RF Level < 0dBm)	$\leq 1.4:1$ (14.0 dB RL), TYP
Connector	SMA

RF Output Frequency

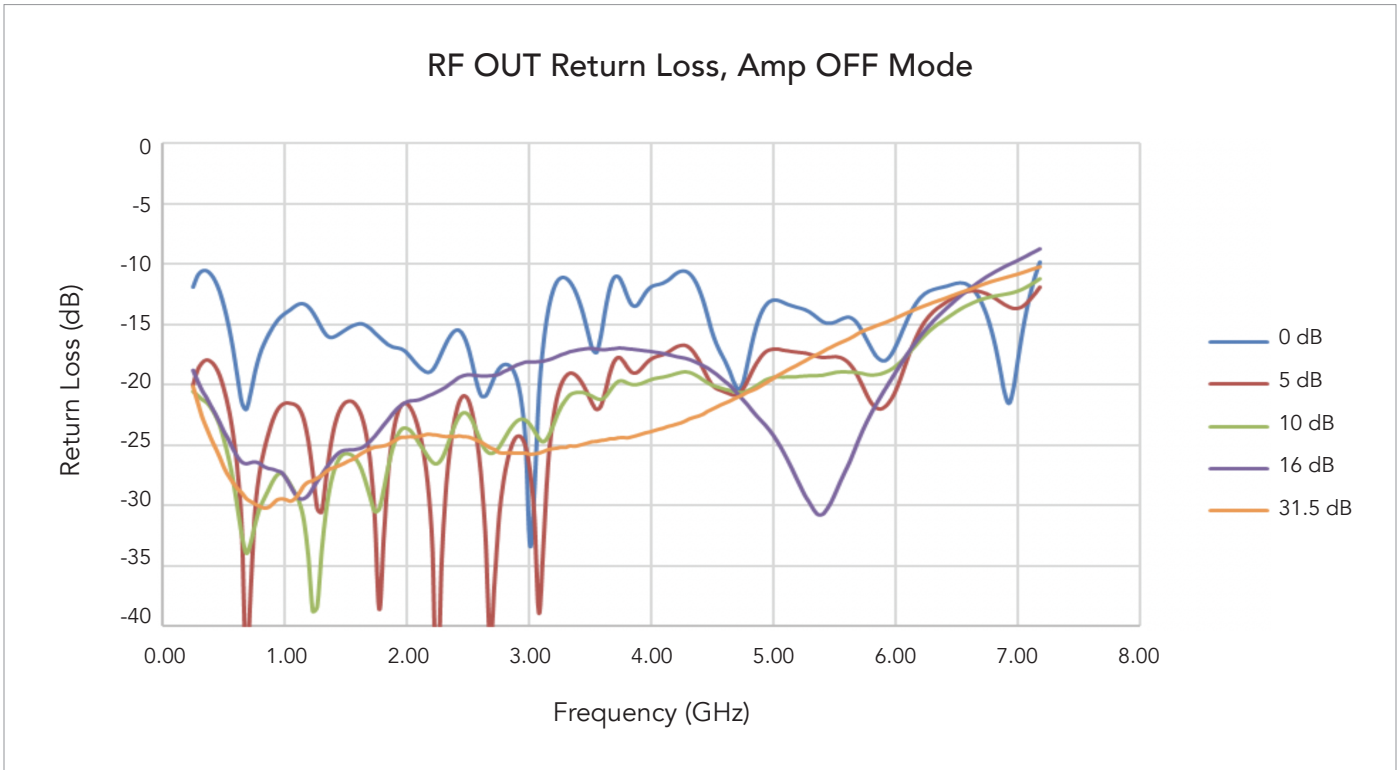
Specification	Value
Output Frequency Range	250 MHz to 7.2 GHz, nominal to 7.5 GHz
Output Frequency Resolution	1 Hz
Output Frequency Switching Speed	≤ 2.5 ms, end-to-end

RF Output Level

Specification	Value: 0.35 GHz to 6.0 GHz	Value: 6.0 GHz to 7.2 GHz
Output Level Control Range	-120 dBm to +20 dBm	
Output Level Control Resolution	0.01 dB	
Output Absolute Level Accuracy (25° C Ambient) RF Level +10 dBm to -80 dBm RF Level -80 dBm to -105 dBm RF Level -105 dBm to -120 dBm	$\leq \pm 0.5$ dB $\leq \pm 0.75$ dB $\leq \pm 1.5$ dB	$\leq \pm 0.75$ dB $\leq \pm 1.0$ dB $\leq \pm 2.0$ dB
Digital Scaling of Output Level	0 to -20 dB usable range 0.01 dB relative accuracy 0.01 dB resolution (up to -3 dB) 0.08 dB resolution (up to -20 dB)	
Output Level Switching Speed	≤ 1 ms, end-to-end (Output AMP OFF) ≤ 2.5 ms, end-to-end (Output AMP ON)	

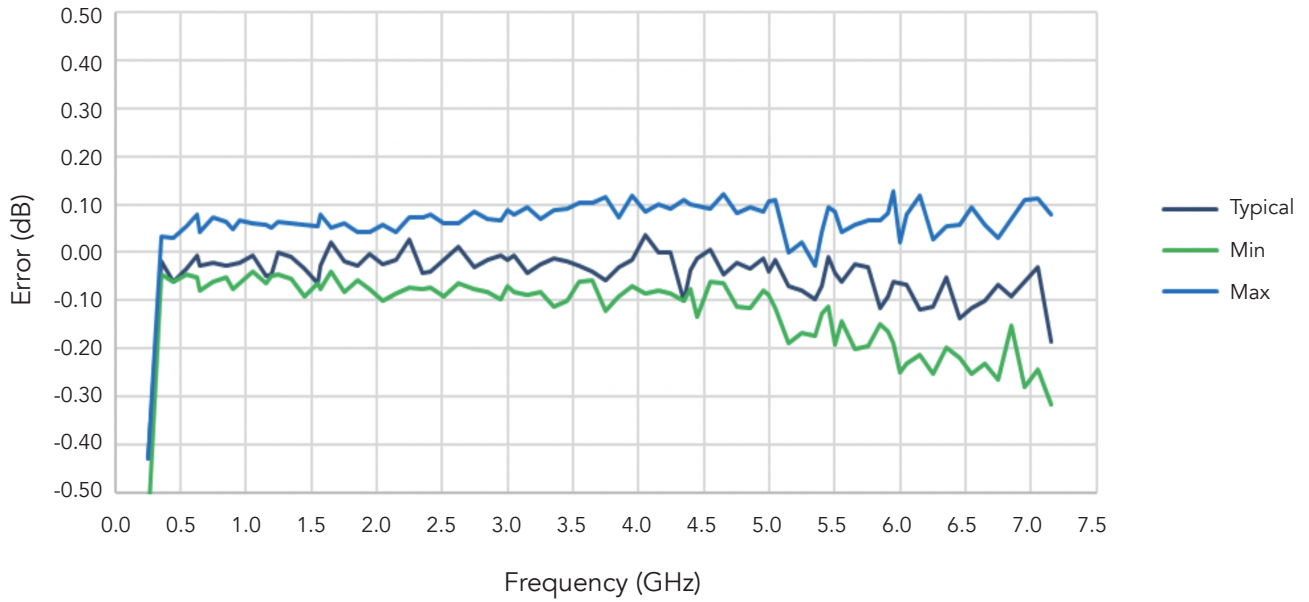


Typical RF Output Return Loss with Output Amp ON

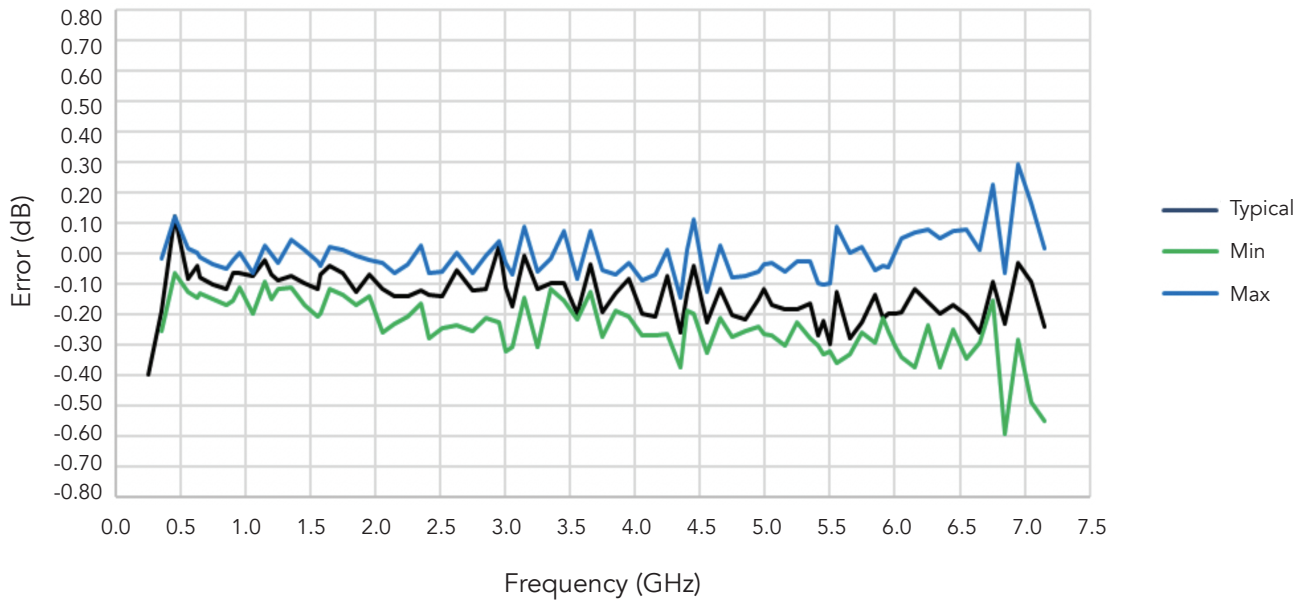


Typical RF Output Return Loss with Output Amp OFF (Bypassed)

Absolute RF Level Accuracy: +5.0 dBm

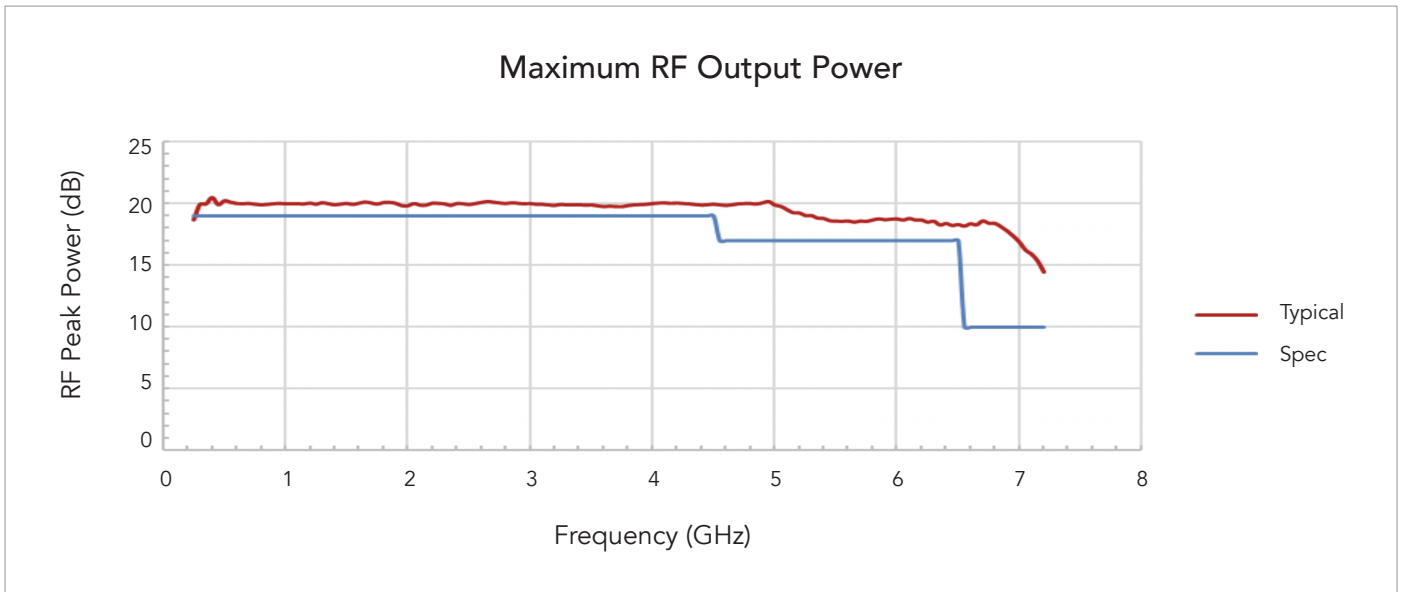


Absolute RF Level Accuracy: -20.0 dBm



Maximum RF Output Level

Specification	Value
Max Levelled RF Output Power (Peak Power)	
250 MHz to 4500 MHz	+19 dBm
4500 MHz to 6500 MHz	+17 dBm
6500 MHz to 7200 MHz	+10 dBm



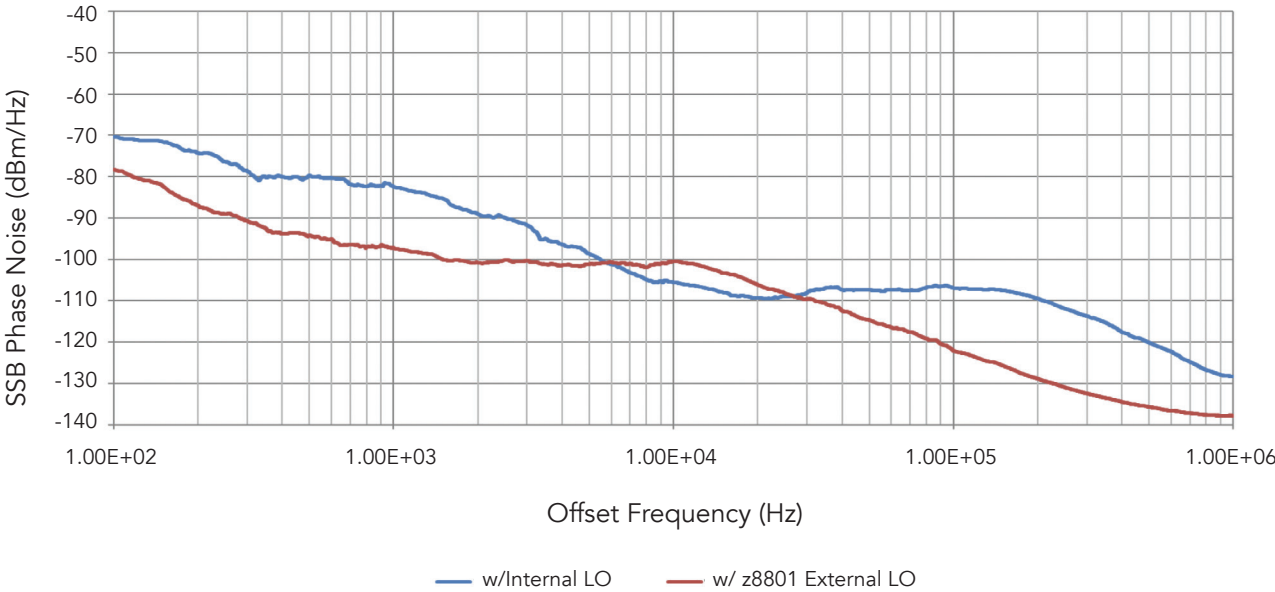
RF Output Instantaneous IF Bandwidth

Specification	Value
IF Modulation Bandwidth (-3 dB)	Up to 500 MHz ($f_0 \pm 250$ MHz)
IF Magnitude Flatness ($f_0 \pm 225$ MHz)	$\leq \pm 1$ dB
IF Phase Linearity ($f_0 \pm 225$ MHz)	$\leq \pm 2^\circ$

RF Output Dynamic Performance

Specification	Value
Spurious-Free Dynamic Range (excluding harmonics)	≥ 75 dBc
Third-Order Intermodulation Distortion (IM3)	≥ -60 dBc
RF Output Harmonics	≤ -40 dBc

z8752 Phase Noise at 5.8 GHz Carrier Frequency (Typical)



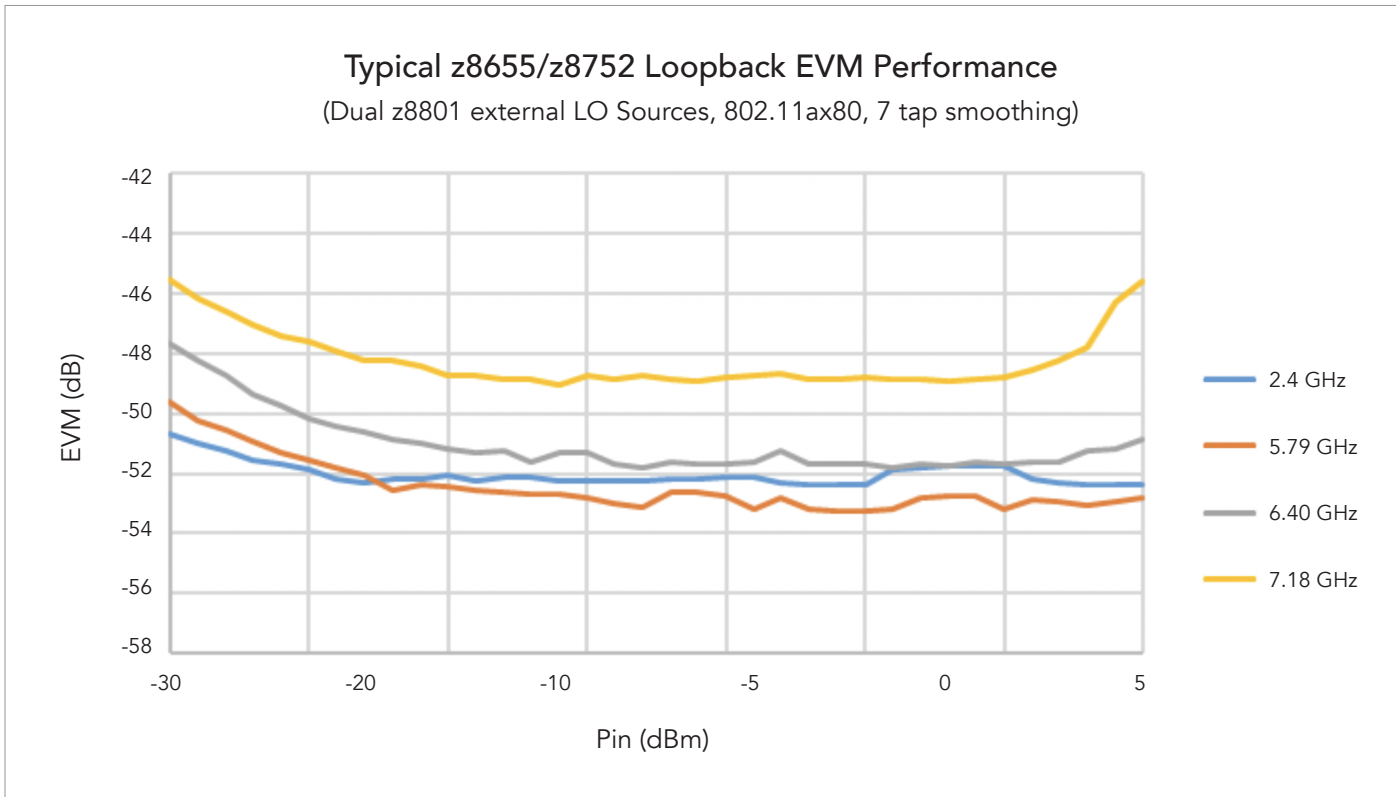
RF Output Single Sideband (SSB) Phase Noise

WLAN Modulation Analysis

IEEE 802.11a/b/g/n/ac/ax OFDM

Residual EVM (Typical), z8801 external LO, w/540Mhz IF offset z8655 VSA measured in loopback w/z8752 VSG

Modulation Bandwidth	EVM Value				
	RF 2.412 GHz	RF 4.80 GHz	RF 6.00 GHz	RF 7.00 GHz	RF 7.125 GHz
20 MHz	-55 dB	-56 dB	-55 dB	-54 dB	-53 dB
40 MHz	-53 dB	-54 dB	-52 dB	-51 dB	-50 dB
80 MHz	-51 dB	-51 dB	-50 dB	-49 dB	-48 dB
160 MHz	-46 dB	-46 dB	-44 dB	-43 dB	-43 dB



Local Oscillator Input

Local Oscillator (LO) Input Channel

Reference Level	Value
LO Channel	One single-ended input, LO IN
Input Impedance	50 Ω , nominal
Input VSWR **	$\leq 2:1$, 250 MHz to 7.2 GHz
Connector	SMA
Expected Input Level	+4 dBm nominal, ± 3 dB

I/Q Output Voltage and Current

Reference Level	Value
Absolute Maximum Output (no damage)** Single-ended Voltage (no load) Differential Voltage (no load) Output Current	± 5 V ± 10 Vd Indefinite Short to Ground
Output Voltage Limit (no clipping) Single-ended (no load) Differential (no load)	± 3 V ± 6 Vd
Output Voltage Ranges Single-ended (no load) Differential (no load)	40 mVpp to 4 Vpp 80 mVppd to 8 Vppd
Output Voltage Range Adjustment Resolution Single-ended (no load) Range: 250 mVpp to 4 Vpp Range: 80 mVpp to 250 mVpp Differential (no load) Range: 500 mVppd to 8 Vppd Range: 80 mVppd to 500 mVppd	0.05% 250 μ V 0.1% 500 μ V
Output Voltage Range Accuracy (no load) 80 mVppd to 8 Vppd Temperature Coefficient (per $^{\circ}$ C)**	$\leq \pm (0.1\% + 1$ mV) $\leq \pm 0.005\%$ of range
Output Current** Linear Operation Maximum (outputs short circuited)	± 50 mA ± 200 mA

I/Q Output DC Offset Adjustment

Reference Level	Value
Output Common Mode Offset Adjustment (no load) Resolution	± 3.0 V 100 μ V resolution
Output Common Mode Offset Accuracy (no load) CM Offset ≤ 3.0 V Temperature Coefficient (per $^{\circ}$ C)**	$\leq \pm 500$ μ V $\leq \pm 0.005\%$ of offset
Output Differential Offset Adjustment (no load) Resolution	± 1 V 35 μ V
Output Differential Offset Accuracy (no load) Diff Offset ≤ 0.98 V Diff Offset > 0.98 V Temperature Coefficient (per $^{\circ}$ C)**	$\leq \pm 500$ μ V $\leq \pm 5$ mV $\leq \pm 0.0025\%$ of offset

I/Q Output Frequency Response

Reference Level	Value
Analog Bandwidth, I or Q Passband Flatness (± 0.5 dB) -3 dB Bandwidth Stopband Rejection	DC to 165 MHz DC to 250 MHz ≥ 50 dB at 500 MHz
I/Q Complex Modulation Bandwidth -3 dB Bandwidth	up to 500 MHz
I/Q Channel-to-Channel Isolation DC to 80 MHz DC to 165 MHz > 165 MHz	≥ 70 dB ≥ 60 dB ≥ 55 dB
I/Q Channel-to-Channel Match, DC to 100 MHz Magnitude Time Skew	$< \pm 0.05$ dB, $< \pm 0.01$ dB typical $< \pm 25$ ps, $< \pm 10$ ps typical

I/Q Output Dynamic Performance

Specification	Limit Value	Typical Value
Spurious-Free Dynamic Range (excluding harmonics) 10.7 MHz, 100 Ω load		
2 Vppd	≥ 74 dBc	81 dBc
1 Vppd	≥ 69 dBc	77 dBc
500 mVppd	≥ 64 dBc	73 dBc
200 mVppd	≥ 60 dBc	67 dBc
100 mVppd	≥ 58 dBc	65 dBc
40 mVppd	≥ 52 dBc	61 dBc
Total Harmonic Distortion (2 nd - 6 th harmonics) 1.8 Vppd, 100 Ω load		
1 MHz	≥ 71 dBc	78 dBc
10.7 MHz	≥ 72 dBc	78 dBc
20.7 MHz	≥ 70 dBc	73 dBc
40.7 MHz	≥ 62 dBc	65 dBc
80.7 MHz	≥ 55 dBc	60 dBc
Third-Order Intermodulation Distortion (IM3) two-tones ± 100 kHz, 10.7 MHz, 100 Ω load		
1 Vppd per tone	≥ 66 dBc	77 dBc
500 mVppd per tone	≥ 71 dBc	83 dBc
250 mVppd per tone	≥ 76 dBc	88 dBc
100 mVppd per tone	≥ 78 dBc	91 dBc
50 mVppd per tone	≥ 87 dBc	101 dBc
20 mVppd per tone	≥ 90 dBc	106 dBc
Output Noise Floor	≤ -142 dBm/Hz	-144 dBm/Hz
Phase Noise at 10.7 MHz, Internal Timebase		
1 kHz offset (PXI)	≤ -110 dBc/Hz	-119 dBc/Hz
1 kHz offset (PXIe)	≤ -110 dBc/Hz	-113 dBc/Hz
10 kHz offset	≤ -125 dBc/Hz	-127 dBc/Hz
100 kHz offset	≤ -128 dBc/Hz	-130 dBc/Hz
1 MHz offset	≤ -127 dBc/Hz	-129 dBc/Hz

I/Q Digital-to-Analog Converter (DAC)

Reference Level	Value
DAC Configuration	Simultaneous Sampling Dual DAC
DAC Vertical Resolution	16 bits 0.0015% of Full-Scale Range
DAC Clock Frequency (simultaneous I/Q sampling)	1 GS/s 2x or 4x DAC interpolation
DAC Clock Jitter**	≤ 500 fs rms
I/Q Data Rate (simultaneous I & Q)	250 MS/s or 500 MS/s
I/Q Data Memory Total Memory Memory per I/Q Channel	512 MiByte total, 128 MiSample (134,217,724 Samples)
I/Q Waveform Size (matched I/Q sizes)	16 Sample to 128 MiSample 4 Sample resolution
I/Q Waveform Types	DC, Sine, Arbitrary
I/Q Center Frequency	DC to ±500 MHz
I/Q Phase Adjustment (I to Q)	± 26.5°, π/6 radians
I/Q Delay Adjustment (I to Q)	± 70 ps
Phase Rotation Range	0 to 360 degrees
Phase Rotation Resolution	0.005 degrees

Timebase Reference

Reference Level	Value
Timebase Frequency	100 MHz or 10 MHz
Timebase Source	Internal TCXO, External Input (front panel), PXI/PXIe Backplane
Internal TCXO Timebase Accuracy	≤ ±2.5 ppm
Timebase Output (10 MHz only)	External Output (front panel)

Modes of Operation

Arbitrary Waveforms Only

Reference Level	Value
Operation Mode Continuous Burst	Generate waveform continuously Generate waveform once
Trigger Mode Immediate Triggered	Start immediately Start upon trigger event
Stop Mode Immediate (hard stop) Upon end of waveform (soft stop)	Stop immediately Stop at end of waveform

Trigger

Reference Level	Value
Trigger Source	External Input (front panel), PXI/PXIe Backplane Trigger 0-7, PXI/PXIe Backplane Star Trigger, Internal Trigger, Software
Trigger Edge	Rising or Falling
Trigger Delay (programmable delay between trigger and waveform start)	0 ns to 30 s 8 ns resolution (excluding trigger latency)
Trigger Re-arm Time (minimum)**	≤ 3 μs
Trigger Latency (trigger event to output on) ** Average Latency (500 MS/s) Average Latency (250 MS/s) Jitter (500 MS/s) Jitter (250 MS/s)	448 ns 702 ns ≤ 17 ns peak-to-peak ≤ 32 ns peak-to-peak
Internal Trigger (programmable period, synchronous to sample clock)	8 ns to 34.36 s period (125 MHz to 0.029 Hz rep rate) 8 ns resolution

Marker Outputs

Reference Level	Value
Marker Channels	Two independent digital outputs
Functionality	Trigger Event, Frame Clock, Symbol Clock, Programmable Time Marker
Output Routing	External Output (front panel), PXI/PXIe Backplane Trigger 0-7
Programmable Time Marker	User-selectable time and width
Marker to Output Latency (marker at point 0)** Average Latency (500 MS/s) Average Latency (250 MS/s) Jitter	3.2 ns 2.0 ns < 0.25 ns

External Input (front panel)

Reference Level	Value
Functionality	Trigger Input, Timebase Reference Input
Absolute Maximum Input (no damage)	$\leq \pm 5 \text{ V}$ (DC + peak AC), CAT I
Input Trigger Level Adjustment	-2 V to +2 V 0.5 mV resolution $\leq 20 \text{ mV}$ accuracy 20 mV overdrive (input hysteresis)
Input Bandwidth (-3 dB)	$\geq 250 \text{ MHz}$
Input Impedance	$1 \text{ M}\Omega \parallel 30 \text{ pF}$ or 50Ω $\leq \pm 2\%$ accuracy
Connector	SMB

External Output (front panel)

Reference Level	Value
Functionality	Trigger Output, Event Output, Marker Output, Timebase Reference Output, Programmable Clock Output, Programmable Pulse Output, Constant Level, Trigger Sync (PA Enable)
Output Event Source	Trigger Event, Waveform Complete Event
Polarity	High or Low Truth
Programmable Event Pulse Width	50 ns to 163 ms
Programmable Clock	Period: 26.667 ns to 100 seconds 13.333 ns resolution 50% Duty Cycle
Programmable Pulse Pulse Repetition Interval Pulse Width	16 ns to 65.5us (sync/ marker) 4 ns resolution (sync/ marker)
Output Level	Programmable Level: Default: +3.3V into open load Open load: 0 to +5V 50 Ω load: 0 to +4.1V Level accuracy: $\pm 5\%$ of FSR Output Drive: $\geq \pm 90$ mA
Output Enable	Tri-State Output Capability
Current Sense	± 90 mA current sense range Triggered or immediate capture 0.1mA resolution
Connector	SMB

Digital Input/Output (DIO) Front Panel¹

Reference Level	Value
Functionality	4-bit bi-directional Digital I/O software programmable. Supports serial interfaces such as MIPI, SPI, I2C, etc.
Programmable Clock Rate	Up to 125MHz
Programmable Logic	≥ 5 ns resolution
Programmable Direction	Input (52 kΩ pull-down) or Output
Programmable Source/Destination	Backplane triggers, external in/out, trigger event
Output Level	Programmable Level: Default: +1.2V into open load Range: +1.2V to +3.6V into open load Level accuracy: ±5%
Output Drive	≥ ±3 mA @ 1.2V ≥ ±8 mA @ 1.8V ≥ ±12 mA @ 3.6V
Output Enable	Tri-State Output Capability
Connector	8-pin Latching Header

Backplane Trigger 0-7

Reference Level	Value
Functionality	Multi-Instrument Synchronization Trigger, Marker
Direction	Input or Output
Polarity	High or Low Truth
Programmable Pulse Width (Trigger & Markers)	16 ns to 65.5 μs 4 ns resolution

Instrument Stored States

Reference Level	Value
Functionality	Non-volatile storage of instrument setup configuration
Stored States	30 State 0 is Reset State Power-On State programmable

¹ DIO connector available only on PXIe product revision 3 and later.

LED Indicators

Reference Level	Value
RDY (Ready)	OFF: Hardware failure ON: Passed power-up self-test TOGGLE: Error pending in queue
TRG (Trigger)	OFF: Trigger event not detected ON/PULSE: Trigger Event Detected

PXle Interface

Reference Level	Value
PCIe Bus Data Interface	x1 single-lane PCIe 250 MByte/s burst, up to 200 MByte/s sustained ²
PCIe Standard Compatibility	Version 1.1
PXle Slot Compatibility	PXle Standard Slot and PXle Hybrid Slot Compatible
PXI Timing & Triggering Signals (XJ4 Connector)	PXI_TRIG[0:7] input/output PXI_STAR input PXI_CLK10 input
PXle Timing & Triggering Signals (XJ3 Connector)	PXle_DSTARA input PXle_CLK100 input PXle_SYNC100 input
PCI Identification Primary ID Secondary ID	3712 (0E80 ₁₆) 8550 (2166 ₁₆)

Power & Cooling

Power Supplies

Platform	Voltage	Typical Current	Maximum Current
PXle	+3.3 VDC +12 VDC	1.26 A 1.31 A	1.41 A 1.58 A

Total Cooling & Power Consumption

Platform	Typical Cooling & Power	Maximum Cooling & Power
PXle	22.6 W	24.2 W

² Sustained PXle transfer rates are dependent upon host system configuration.

Physical & Environmental

Size & Weight

Specification	Value
Physical size	Double-Wide 3U PXIe Instrument
Dimensions (L x W x H)	8.25 in. x 1.59 in. x 5.25 in. 20.96 cm x 4.03 cm x 13.34 cm
Weight	27.1 oz. or 0.768 kg

Temperature Range

Specification	Value
Operating	0 °C to +50°C ambient (MIL-PRF28800F Class 3)
Storage	-40 °C to +75 °C ambient (MIL-PRF28800F Class 3)
Calibration Range	+20 °C to +30 °C ambient, after 20 minute warm-up period, to meet all specification accuracies
Calibration Interval	12 Months from calibration date
Over-Temperature	Automatic shutdown if internal temperature exceeds +65 °C

Relative Humidity

Specification	Value
Operating or Storage Up to +30°C +30°C to +40°C above +40 °C	5 to 95 ± 5%, non-condensing 5 to 75 ± 5%, non-condensing 5 to 45 ± 5%, non-condensing

Altitude

Specification	Value
Operating	Up to 5 km
Storage	Up to 15 km

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